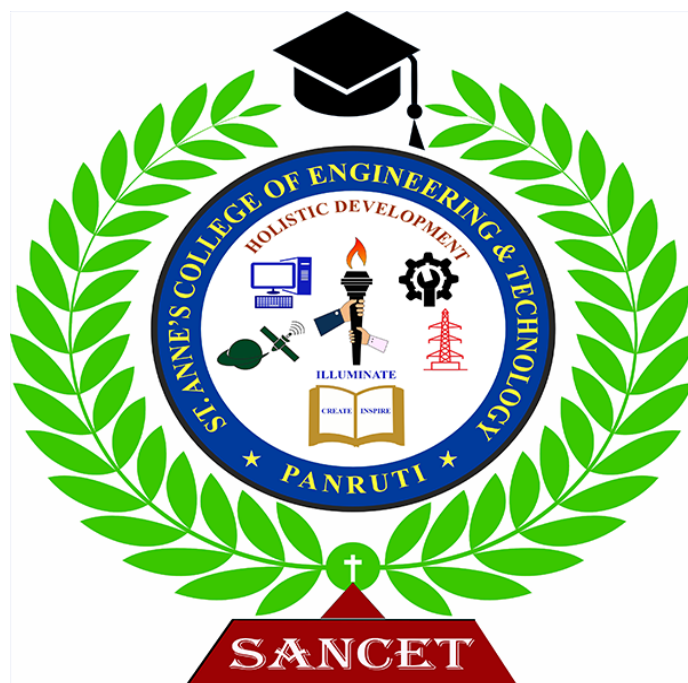


ST. ANNE'S

COLLEGE OF ENGINEERING & TECHNOLOGY

ANGUCHETTPALAYAM, PANRUTI
Cuddalore District – 607 110.



EC 8311 – ELECTRONICS LABORATORY

NAME :
REGISTER NO. :
COURSE : B.E.
BRANCH : ELECTRICAL AND ELECTRONICS
ENGINEERING
YEAR & SEM : II YEAR & III SEM

EC8311 - ELECTRONICS LABORATORY

L	T	P	C
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OBJECTIVES:

To enable the students to understand the behavior of semiconductor device based on experimentation.

LIST OF EXPERIMENTS

1. Characteristics of Semiconductor diode and Zener diode.
2. Characteristics of a NPN Transistor under common emitter, common collector and common base configurations.
3. Characteristics of JFET and draw the equivalent circuit.
4. Characteristics of UJT and generation of saw tooth waveforms.
5. Design and Frequency response characteristics of a Common Emitter amplifier.
6. Characteristics of photo diode & photo transistor, Study of light activated relay circuit.
7. Design and testing of RC phase shift and LC oscillators.
8. Single Phase half-wave and full wave rectifiers with inductive and capacitive filters.
9. Differential amplifiers using FET.
10. Study of CRO for frequency and phase measurements.
11. Realization of passive filters.

TOTAL: 60 PERIODS

OUTCOMES:

Ability to understand and analyze Electronic Devices and Circuits.

CYCLE – I

1. Study of CRO for frequency and phase measurements
2. Characteristics of Semiconductor diode and Zener diode
3. Characteristics of a NPN Transistor under common emitter , common collector and common base configurations
4. Characteristics of JFET and draw the equivalent circuit
5. Characteristics of UJT and generation of saw tooth waveforms
6. Design and Frequency response characteristics of a Common Emitter amplifier

CYCLE – II

7. Characteristics of photo diode & photo transistor, Study of light activated relay circuit
8. Design and testing of RC phase shift and LC oscillators
9. Single Phase half-wave and full wave rectifiers with inductive and capacitive filters
10. Differential amplifiers using FET
11. Realization of passive filters

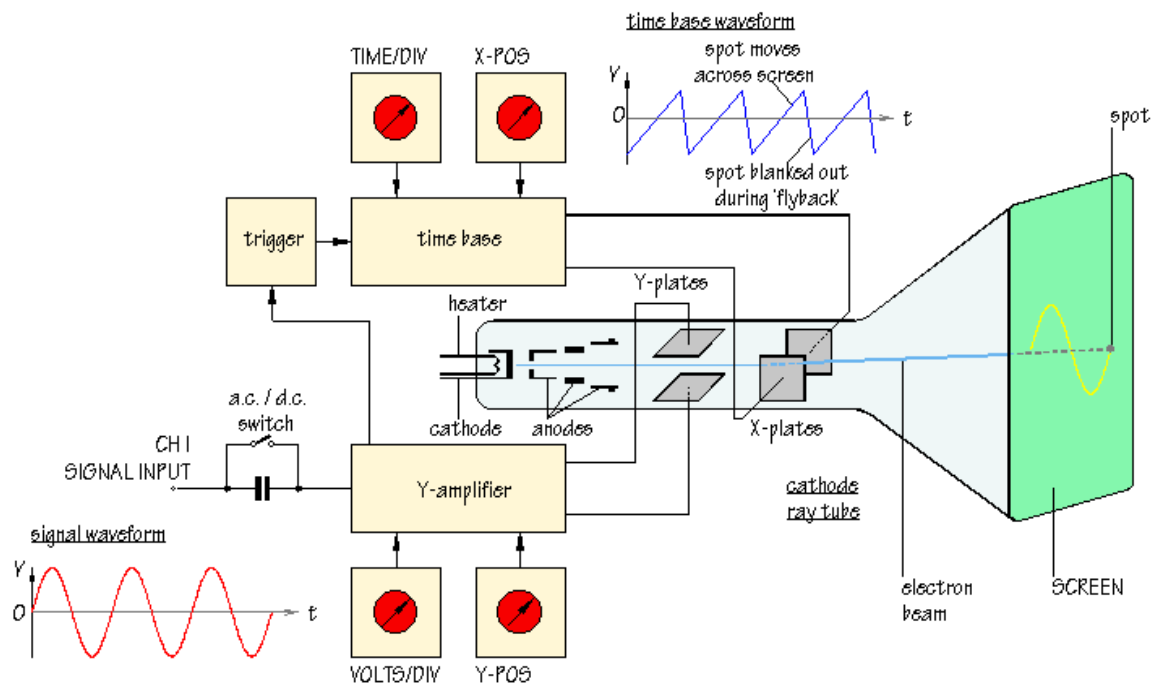
TOPIC BEYOND SYLLABUS

12. Tuned class C Amplifier

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	b) Characteristics of Zener diode	19
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4	Characteristics of JFET and its equivalent circuit	41
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Block Diagram of CRO



Observation

Function	Vertical Division (a)	Volt/div (b)	Amplitude (p-p) $V = a * b$	Horizontal Div. (c)	Time/div (d)	Time (Period) $T = c * d$	Freq. $F = 1/T$
Sine wave							
Square Wave							
Triangular Wave							

Ex. No.: 1

**STUDY OF CRO FOR FREQUENCY AND PHASE
MEASUREMENTS**

AIM:

To observe sine wave, square wave and triangular waveforms on the Cathode Ray Oscilloscope and to measure amplitude, frequency and Phase of the waveforms.

APPARATUS REQUIRED:

Sl. No	Components / Equipments	Specifications	Quantity
1	CRO-Cathode Ray Oscilloscope	20 MHz	1
2	Function Generator	1MHz	1
3	BNC CRO Probes		3

THEORY:

CRO-(Cathode Ray Oscilloscope) is the instrument which is used to observe signal waveforms. Signals are displayed in time domain i.e. variation in amplitude of the signal with respect to time is plotted on the CRO screen. X-axis represents time and Y-axis represents amplitude. It is used to measure amplitude, frequency and phase of the waveforms. It is also used to observe shape of the waveform. C.R.O. is useful for troubleshooting purpose. It helps us to find out gain of amplifier, test oscillator circuits.

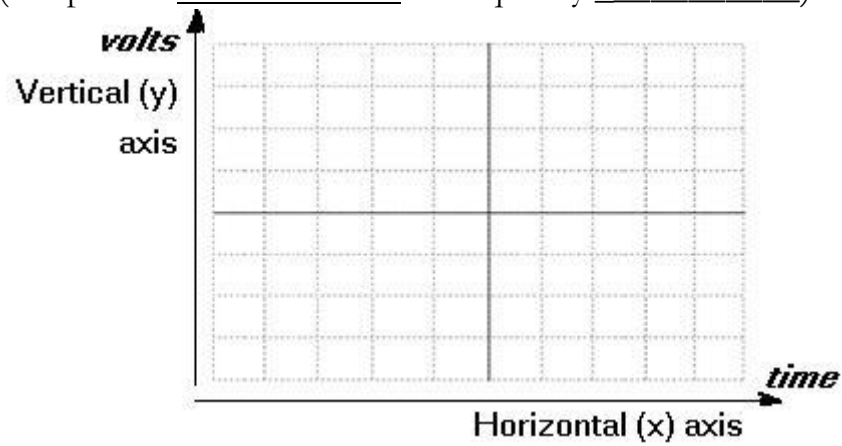
A CRO is a versatile instrument that can be used to measure voltage, time intervals, and the phase angle between two sinusoidal voltages of the same frequency. There are 8 vertical divisions and 10 horizontal divisions indicated with grid lines or graticules. A standard screen size is 8 cm by 10 cm. The screen is coated with phosphor that emits light when struck by the electron beam. We can measure following parameters using the CRO:

- ✓ AC or DC voltage.
- ✓ Time ($t=1/f$).
- ✓ Phase relationship
- ✓ Waveform calculation: Rise time; fall time; on time; off-time Distortion, etc.

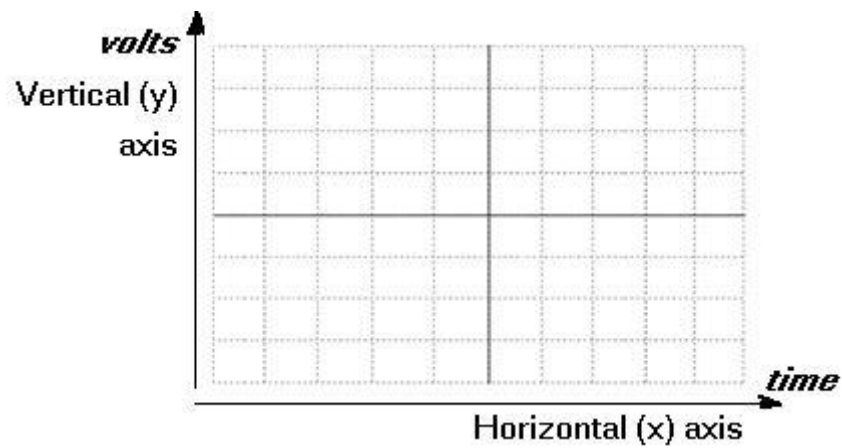
Latest digital storage oscilloscope display voltage and frequency directly on the LCD and does not require any calculations. It can also store waveform for further analysis.

Draw observed waveforms

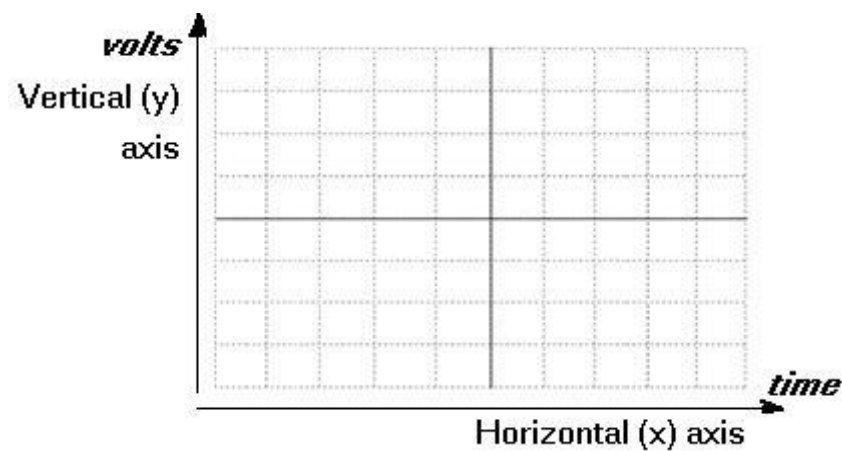
Sine wave: (Amplitude: _____ Frequency _____)



Square Wave: (Amplitude: _____ Frequency _____)



Triangular Wave: (Amplitude: _____ Frequency _____)



Major blocks:

- ✓ Cathode ray tube (CRT)
 - Electron gun assembly
 - Deflection plate unit
 - Screen.
- ✓ Vertical amplifier
- ✓ Horizontal amplifier
- ✓ Sweep generator
- ✓ Trigger circuit
- ✓ Associated power supply.

FORMULA:

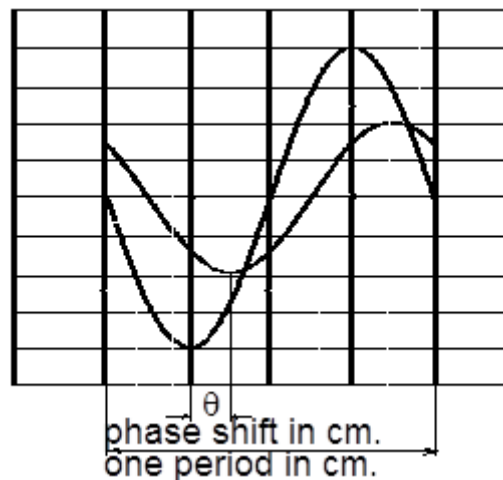
Amplitude = No. of vertical divisions * Volts/div.

Time period = No. of horizontal divisions * Time/div.

Frequency = $(1/T)$ Hz

Measurement of Phase

The calibrated time scales can be used to calculate the phase shift between two sinusoidal signals of the same frequency. If a dual trace or beam CRO is available to display the two signals simultaneously (one of the signals is used for synchronization), both of the signals will appear in proper time perspective and the amount of time difference between the waveforms can be measured. This, in turn can be utilized to calculate the phase angle θ , between the two signals.



Referring to figure.1, the phase shift can be calculated by the formula;

$$\theta = \frac{\text{Phase shift in cm.}}{\text{One period in cm.}} \times 360^\circ$$

The frequency relationship between the horizontal and vertical inputs is given by;

$$\frac{f_h}{f_v} = \frac{\text{No. of tangencies (vertical)}}{\text{No. of tangencies (horizontal)}}$$

from which f_v , the unknown frequency can be calculated.

PROCEDURE:

1. Connect function generator output at the input of C.R.O. at channel 1 or at channel 2.
2. Select proper channel i.e. if signal is connected to channel 1 select CH1 and if signal is connected to channel 2 select CH2.
3. Adjust Time /Div. knob to get sufficient time period displacement of the wave on the CRO screen.
4. With fine tuning of time/Div. make the waveform steady on screen.
5. Use triggering controls if waveform is not stable.
6. Keep volt/div knob such that waveform is visible on the screen without clipping.
7. Measure P-P reading along y-axis. This reading multiplied with volt/div gives peak to peak amplitude of the ac i/p wave.
8. Measure horizontal division of one complete cycle. This division multiplied by time/div gives time period of the i/p wave.
9. Calculate frequency using formula $f = 1/T$.
10. Note down your readings in the observation table.
11. Draw waveforms of sine, square, ramp and triangular in the given space.

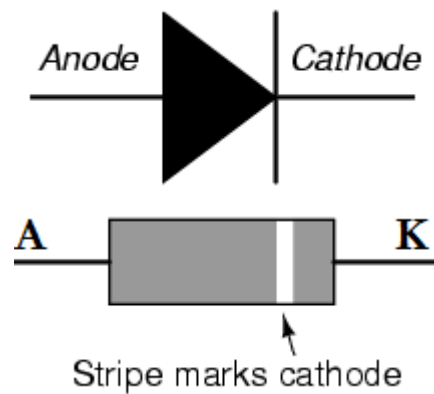
REVIEW QUESTIONS:

1. What is the use of CRO & mention the Manufactures.
2. Define the terms offset error, peak value and peak to peak value.
3. What is the highest frequency that can be measured by CRO available in your laboratory?
4. What is highest voltage that can be measured by CRO available in your laboratory?
5. What you will do to measure voltage which is greater than voltage limit of the CRO?
6. What do you mean by dual channel CRO?
7. What type of deflection mechanism used in CRO to deflect electron beam?
8. How to test whether CRO probe is in working condition or not?
9. How do you measure the frequency and phase angle in CRO?
10. What is the use of AC/DC input coupling push-button switch, Volt/Div. and Time/Div. knob in CRO?

RESULT:

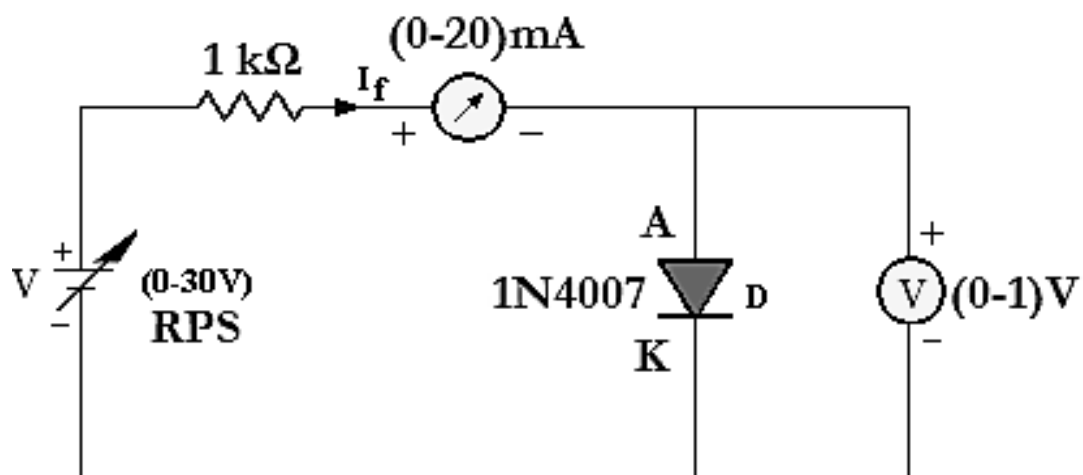
Thus the operation of CRO has been studied along with the measurement of frequency and phase of a signal.

SYMBOL & PIN DIAGRAM:

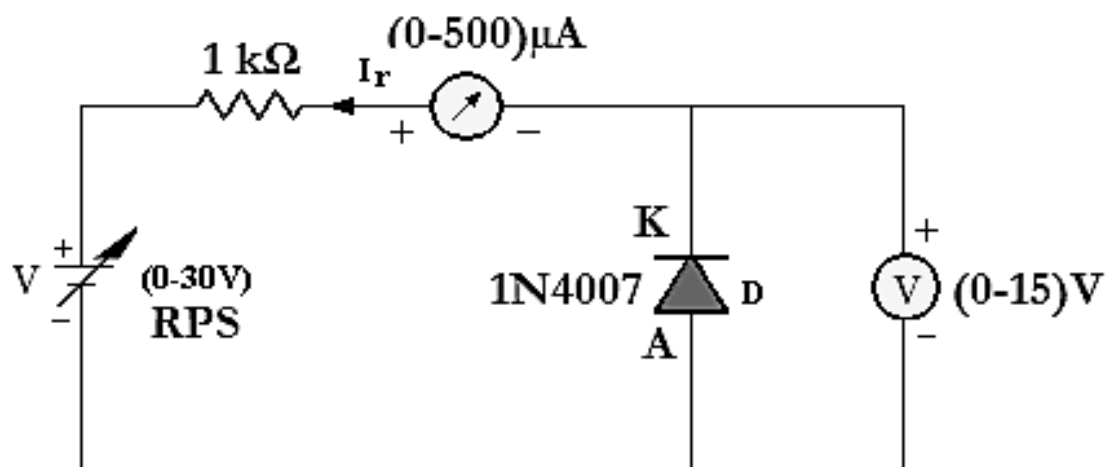


CIRCUIT DIAGRAM:

FORWARD BIAS:



REVERSE BIAS:



Ex. No.: 2(a)

CHARACTERISTICS OF SEMICONDUCTOR PN DIODE

AIM:

To Plot the Volt Ampere Characteristics of PN Junction Diode under Forward and Reverse Bias Conditions, and to find the Cut-in voltage, Static Resistance, Dynamic Resistance under Forward and Reverse Bias.

APPARATUS REQUIRED:

Sl. No	Components / Equipments	Specifications	Quantity
1	Diode- PN	IN4007	1
2	Resistors	1k Ω	1
3	Dual Regulated Power Supply	(0-30)V	1
4	Voltmeters	MC (0-1)V, (0-15)V	Each One
5	Ammeters	MC (0-500) μ A, (0-20) mA	Each One
6	Bread Board		1
7	Connecting Wires		Few

THEORY:

A diode is a PN junction formed by a layer of P type and layer of N type Semiconductors. Once formed the free electrons in the N region diffuse across the junction and combine with holes in P region and so a depletion Layer is developed. The depletion layer consists of ions, which acts like a barrier for diffusion of charged beyond a certain limit. The difference of potential across the depletion layer is called the barrier potential. At 2.5degree the barrier potential approximately equal 0.7v for silicon diode and 0.3v for germanium diode.

When the junction is forward bias, the majority carrier acquired sufficient energy to overcome the barrier and the diode conducts. When the junction is reverse biased the depletion layer widens and the barrier potential increases. Hence the Majority carrier cannot cross the junction and the diode does not conduct. But there will be a leakage current due to minority carrier. When diode is forward biased, resistance offered is zero, and when reverse biased resistance offered is infinity. It acts as a perfect switch.

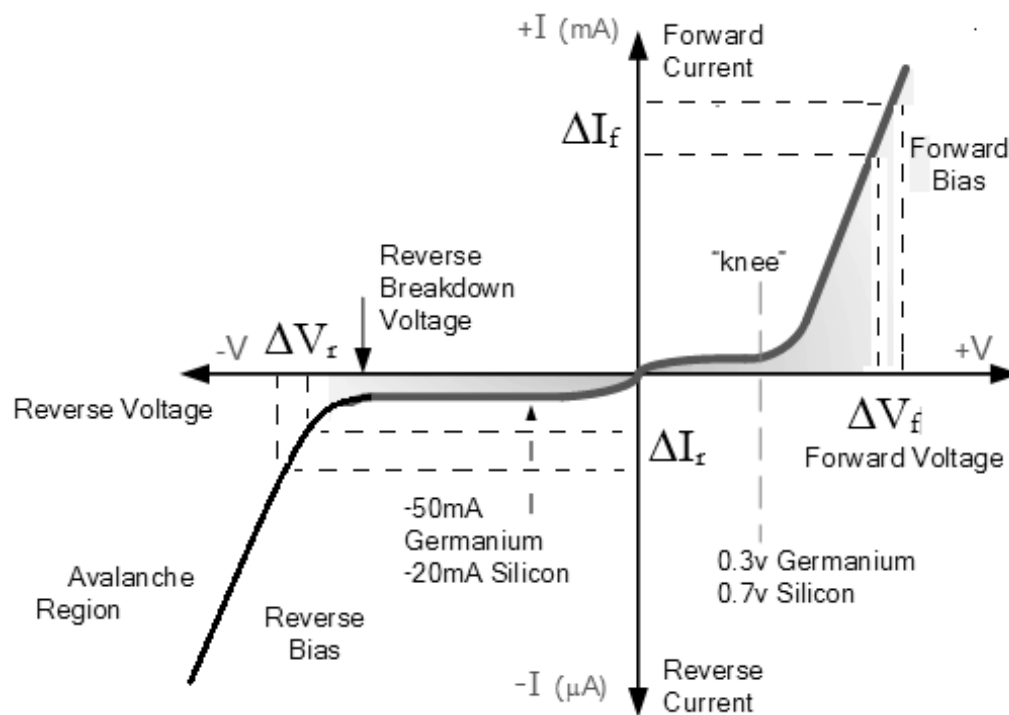
TABULATION:
FORWARD BIAS:

$V_f(\text{volts})$	$I_f(\text{mA})$

REVERSE BIAS:

$V_r(\text{volts})$	$I_r(\text{mA})$

MODEL GRAPH:



PROCEDURE:

FORWARD BIAS:

1. The connections are made as per the circuit diagram.
2. The positive terminal of power supply is connected to anode of the diode and negative terminal to cathode of the diode.
3. Forward voltage V_f across the diode is increased in small steps and the forward current is noted.
4. The readings are tabulated. A graph is drawn between V_f and I_f .

REVERSE BIAS:

1. The connections are made as per the circuit diagram.
2. The positive terminal of power supply is connected to cathode of the diode and negative terminal to anode of the diode.
3. Reverse voltage V_r across the diode is increased in small steps and the Reverse current is noted.
4. The readings are tabulated. A graph is drawn between V_r and I_r .

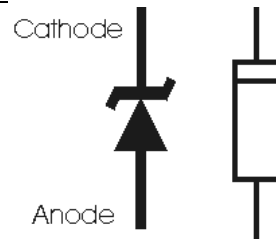
REVIEW QUESTIONS:

1. How a PN junction is formed?
2. In what way the width of depletion region can be varied?
3. What is potential barrier?
4. In forward bias condition the current condition is due to _____
5. What is reverse saturation current I_{co} ?
6. How diodes act as switch?
7. What is Dynamic Resistance?
8. Why it is called as Diode?
9. What are the majority carriers of P-type and N-type semiconductor?
10. What is an ideal diode? How does it differ from a real diode?

RESULT:

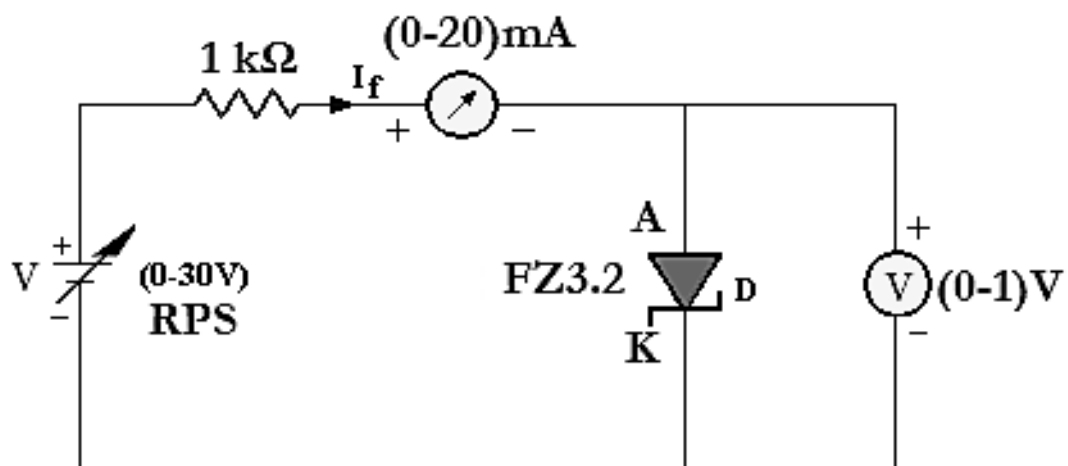
Thus the characteristics of PN diode were drawn and the necessary parameters are calculated from the graph.

SYMBOL & PIN DIAGRAM:

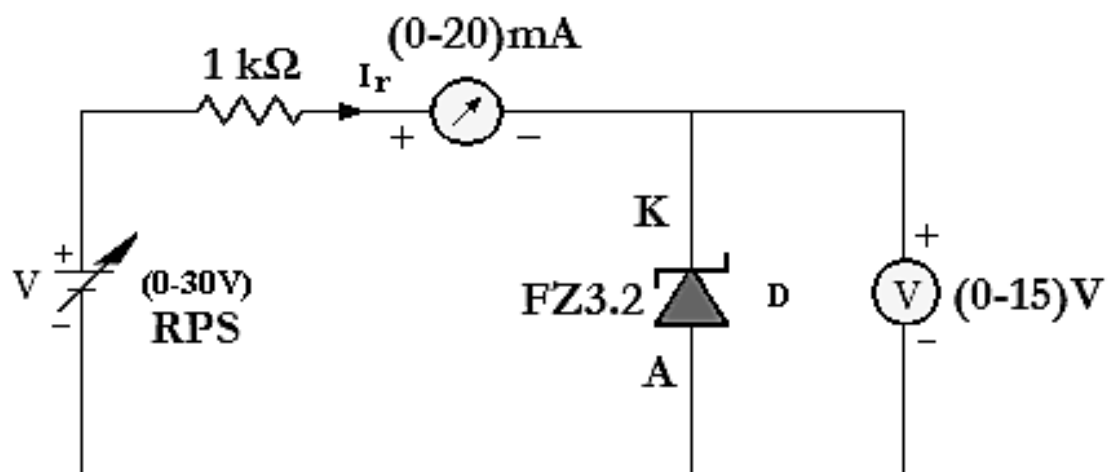


CIRCUIT DIAGRAM:

FORWARD BIAS:



REVERSE BIAS:



Ex. No.: 2(b)

CHARACTERISTICS OF ZENER DIODE

AIM:

To Obtain the Forward Bias and Reverse Bias characteristics of a Zener diode, and to find the Zener Break down Voltage from the Characteristics.

APPARATUS REQUIRED:

Sl. No	Components / Equipments	Specifications	Quantity
1	Diode- Zener	FZ3.2	1
2	Resistors	1k Ω	1
3	Dual Regulated Power Supply	(0-30)V	1
4	Voltmeters	MC (0-1)V, (0-10)V	Each One
5	Ammeters	MC (0-20)mA	1
6	Bread Board		1
7	Connecting Wires		Few

THEORY:

Zener diodes have many of the same basic properties of ordinary semiconductor diodes. When forward biased, they conduct in the forward direction and have the same turn on voltage as ordinary diodes. For silicon this is about 0.6 volts.

In the reverse direction, the operation of a Zener diode is quite different to an ordinary diode. For low voltages the diodes do not conduct as would be expected. However, once a certain voltage is reached the diode "breaks down" and current flows. Looking at the curves for a Zener diode, it can be seen that the voltage is almost constant regardless of the current carried. This means that a Zener diode provides a stable and known reference voltage. Hence they are used as Voltage regulators.

TABULATION:

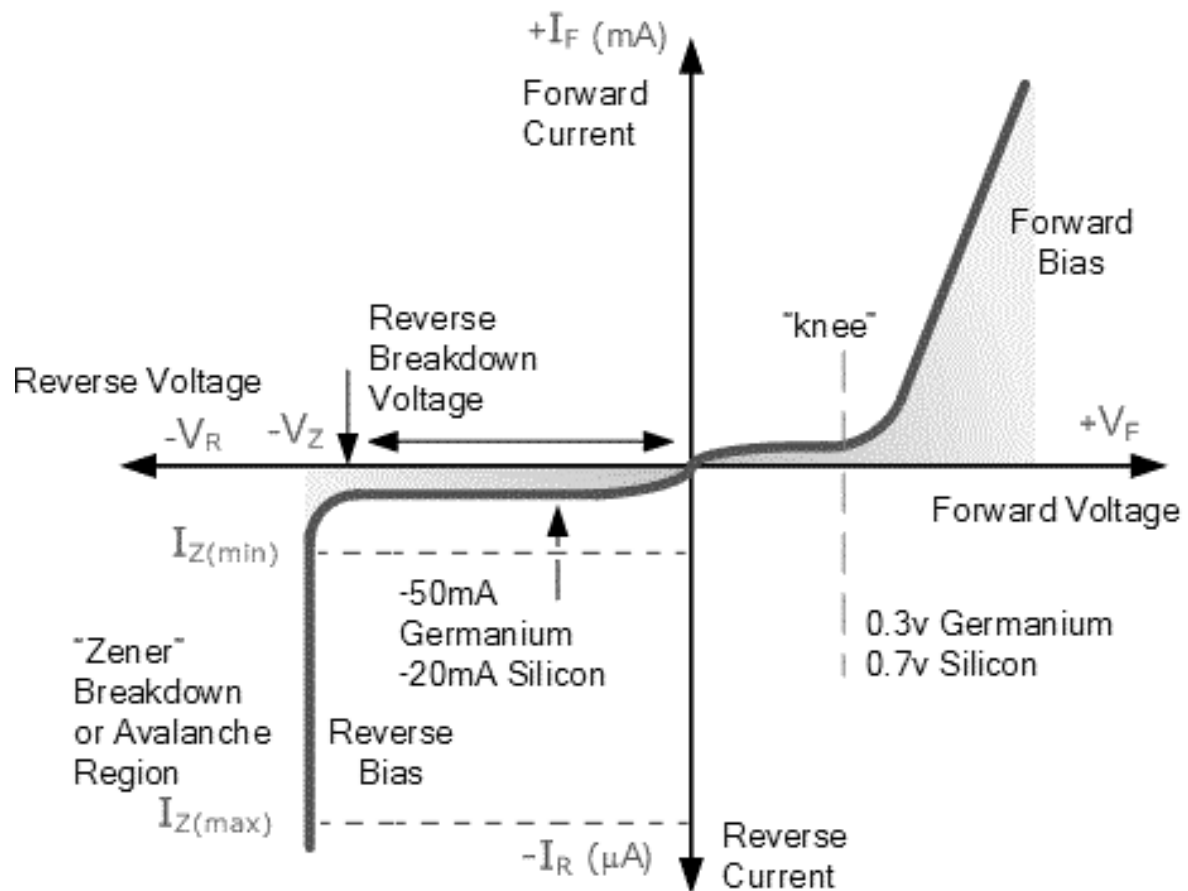
FORWARD BIAS:

$V_f(\text{volts})$	$I_f(\text{mA})$

REVERSE BIAS:

$V_r(\text{volts})$	$I_r(\text{mA})$

MODEL GRAPH:



PROCEDURE:

FORWARD BIAS:

1. The connections are made as per the circuit diagram.
2. The positive terminal of power supply is connected to anode of the diode and negative terminal to cathode of the diode.
3. Forward voltage V_f across the diode is increased in small steps and the forward current is noted.
4. The readings are tabulated. A graph is drawn between V_f and I_f .

REVERSE BIAS:

1. The connections are made as per the circuit diagram.
2. The positive terminal of power supply is connected to cathode of the diode and negative terminal to anode of the diode.
3. Reverse voltage V_r across the diode is increased in small steps and the Reverse current is noted.
4. The readings are tabulated. A graph is drawn between V_r and I_r .

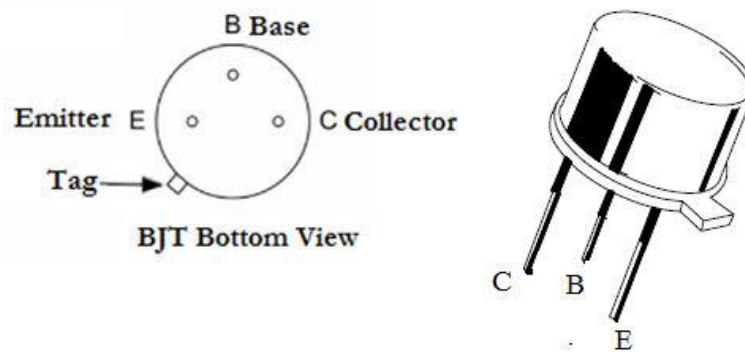
REVIEW QUESTIONS:

1. How Zener diode acts as a voltage regulator?
2. Explain working of a Zener Diode.
3. What is the cut-in voltage of Zener diode?
4. Differentiate between Zener Breakdown and Avalanche breakdown.
5. Why Zener diode is often preferred than PN diode?
6. List the application of Zener diode.
7. Define Zener breakdown voltage.
8. List the other Zener diode with different breakdown voltages.
9. Can we use Zener diode as a switch?
10. What will happens if PN regions are heavily doped in Zener diode?

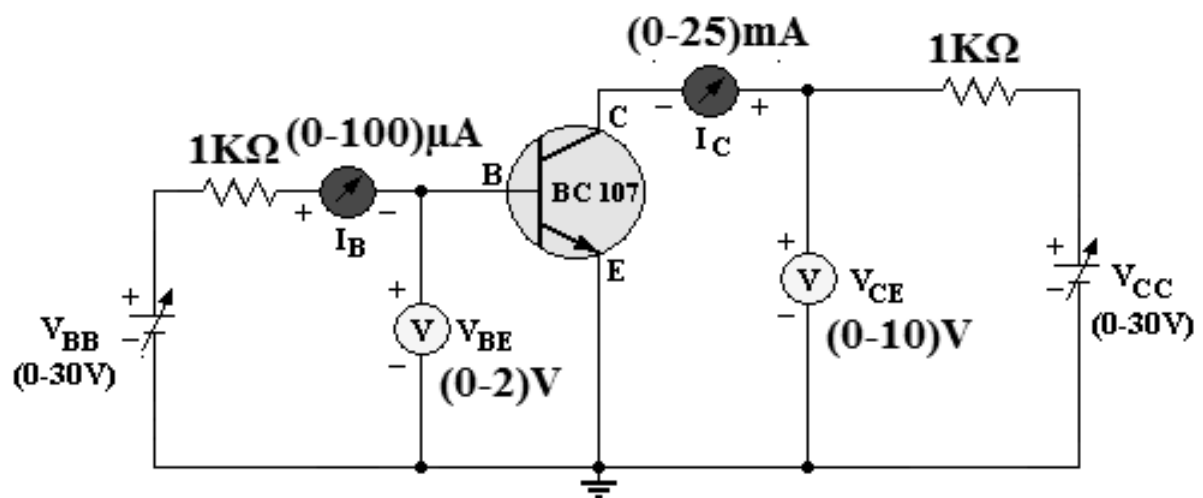
RESULT:

Thus the characteristics of Zener diode were drawn and the necessary parameters are determined from the graph.

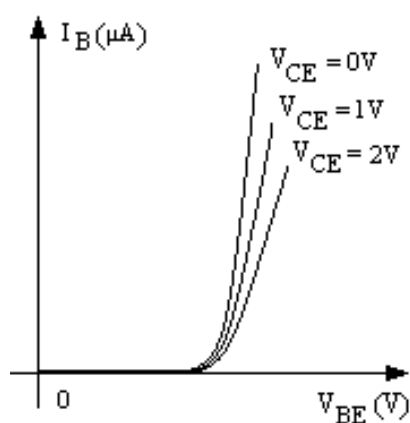
PIN DIAGRAM OF BC107



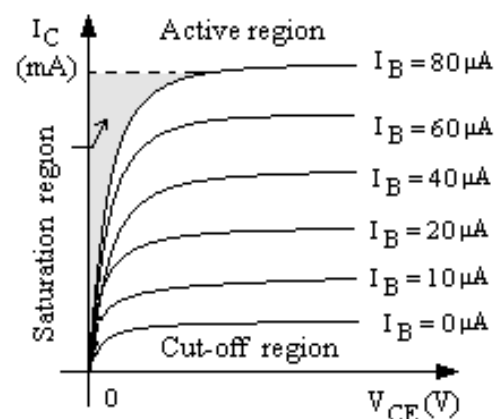
CIRCUIT DIAGRAM: COMMON EMITTER CIRCUIT CHARACTERISTICS:



MODEL GRAPH:



CE I/P Characteristics



CE O/P Characteristics

Ex. No.: 3(a)

**CHARACTERISTICS OF NPN TRANSISTOR UNDER COMMON
EMITTER CONFIGURATION**

AIM:

To plot the Input and Output characteristics of a transistor connected in Common Emitter Configuration and to find the dynamic resistance and amplification factor.

APPARATUS REQUIRED:

Sl. No	Components / Equipments	Specifications	Quantity
1	Transistor BC107	Max Rating : 50V 1A, 3W	1
2	Resistors	1k Ω , (or) 470 Ω	2
3	Dual Regulated Power Supply	(0-30)V	1
4	Voltmeters	MC (0-2)V, (0-10)V	Each One
5	Ammeters	MC (0-25)mA, (0-100) μ A	Each One
6	Bread Board		1
7	Connecting Wires		Few

THEORY:

A Bipolar Junction Transistor or BJT is a three terminal device having two PN-junctions connected together in series. Each terminal is given a name to identify it and these are known as the Emitter (E), Base (B) and Collector (C). There are two basic types of bipolar transistor construction, NPN and PNP, which basically describes the physical arrangement of the P-type and N-type semiconductor materials from which they are made. Bipolar Transistors are "CURRENT" Amplifying or current regulating devices that control the amount of current flowing through them in proportion to the amount of biasing current applied to their base terminal. The principle of operation of the two transistors types NPN and PNP, is exactly the same the only difference being in the biasing (base current) and the polarity of the power supply for each type. In CE configuration, Emitter is common to both the input and output as shown in figure. The direction of the arrow in the symbol shows current flow between the base and emitter terminal, pointing from the positive P-type region to the negative N-type region, exactly the same as for the standard diode symbol. For normal operation, the emitter-base junction is forward-biased and the collector-base junction is reverse-biased.

TABULATION:

INPUT CHARACTERISTICS:

[illegible]

OUTPUT CHARACTERISTICS:

$I_B = \quad \mu A$		$I_B = \quad \mu A$	
$V_{CE} (V)$	$I_C (mA)$	$V_{CE} (V)$	$I_C (mA)$

DESCRIPTION:

Input Characteristics: The variation of the base current I_B with the base-emitter voltage V_{BE} keeping the collector-emitter voltage V_{CE} fixed, gives the input characteristic in C_E mode.

Input Dynamic Resistance (r_i): This is defined as the ratio of change in base emitter voltage (ΔV_{BE}) to the resulting change in base current (ΔI_B) at constant collector-emitter voltage (V_{CE}). This is dynamic and it can be seen from the input characteristic, its value varies with the operating current in the transistor:

$$r_i = \left. \frac{\Delta V_{BE}}{\Delta I_B} \right|_{V_{CE}}$$

The value of r_i can be anything from a few hundreds to a few thousand ohms.

Output Characteristics: The variation of the collector current I_C with the collector-emitter voltage V_{CE} is called the output characteristic. The plot of I_C versus V_{CE} for different fixed values of I_B gives one output characteristic. Since the collector current changes with the base current, there will be different output characteristics corresponding to different values of I_B .

Output Dynamic Resistance (r_o): This is defined as the ratio of change in collector-emitter voltage (ΔV_{CE}) to the change in collector current (ΔI_C) at a constant base current I_B .

$$r_o = \left. \frac{\Delta V_{CE}}{\Delta I_C} \right|_{I_B}$$

The high magnitude of the output resistance (of the order of 100 kW) is due to the reverse biased state of this diode.

Transfer Characteristics: The transfer characteristics are plotted between the input and output currents (I_B versus I_C). Both I_B and I_C increase proportionately.

Current amplification factor (β)

This is defined as the ratio of the change in collector current to the change in base current at a constant collector-emitter voltage (V_{CE}) when the transistor is in active state.

$$\beta_{ac} = \left. \frac{\Delta I_C}{\Delta I_B} \right|_{V_{CE}}$$

This is also known as small signal current gain and its value is very large. The ratio of I_C and

I_B we get what is called dc of the transistor. Hence,

$$\beta_{dc} = \left. \frac{I_C}{I_B} \right|_{V_{CE}}$$

Since I_C increases with I_B almost linearly, the values of both dc and ac are nearly equal.

PROCEDURE:**TO FIND THE INPUT CHARACTERISTICS:**

1. Connect the circuit as in the circuit diagram.
2. Keep V_{BB} and V_{CC} in zero volts before giving the supply
3. Set $V_{CE} = 1$ volt by varying V_{CC} and vary the V_{BB} smoothly with fine control such that base current I_B varies in steps of $5\mu A$ from zero up to $100\mu A$, and note down the corresponding voltage V_{BE} for each step in the tabular form.
4. Repeat the experiment for $V_{CE} = 1$ volt and 2 volts.
5. Draw a graph between V_{BE} vs. I_B against $V_{CE} = \text{Constant}$.

TO FIND THE OUTPUT CHARACTERISTICS:

1. Start V_{EE} and V_{CC} from zero Volts.
2. Set the $I_B = 20\mu A$ by using V_{BB} such that, V_{CE} changes in steps of 0.2 volts from zero up to 10 volts, note down the corresponding collector current I_C for each step in the tabular form.
3. Repeat the experiment for $I_E = 20\mu A$ and $I_E = 40\mu A$, tabulate the readings.
4. Draw a graph between V_{CE} Vs I_C against $I_B = \text{Constant}$.

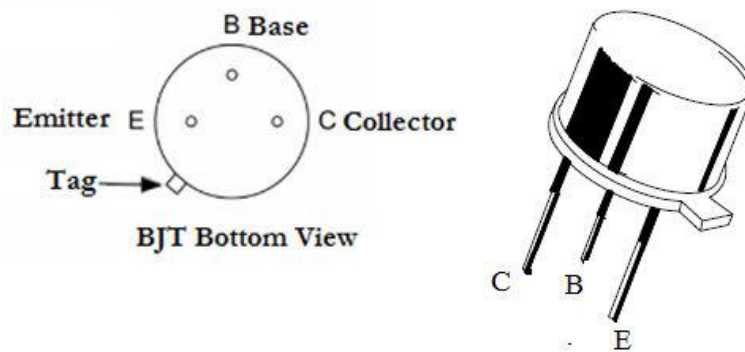
REVIEW QUESTIONS:

1. Why BJT is called current controlled device?
2. Why CE configuration is commonly used for amplifier circuits?
3. Why I_B vs. V_{BE} plots move outwards for higher values of V_{CE} in CE input characteristics?
4. What is indicated by B, C and 107 in BC107?
5. What are the regions of operation of a transistor?
6. Can transistor be replaced by two back to back connected diodes?
7. To operate a transistor as amplifier, emitter junction is forward biased and collector junction is reverse biased. Why?
8. What is the relation between α , β and γ and mention the range of β for BJT?
9. List the current components of BJT in CE configuration.
10. Why the doping of collector is less compared to emitter?
11. What is the difference between CE and emitter follower circuit?
12. What is the phase relation between input and output?
13. Draw diagram of CE configuration for PNP transistor?
14. What is the power gain of CE configuration?
15. What are the applications of CE configuration?

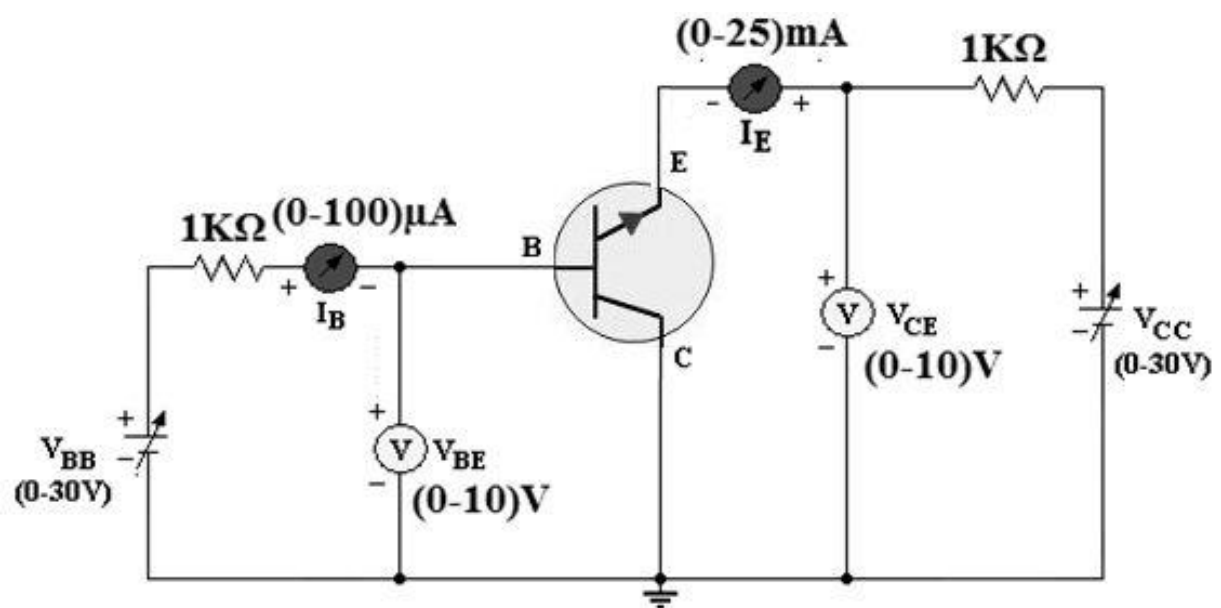
RESULT:

Thus the input and output characteristic of BJT in Common Emitter configuration were plotted and the dynamic resistance and amplification factor were obtained.

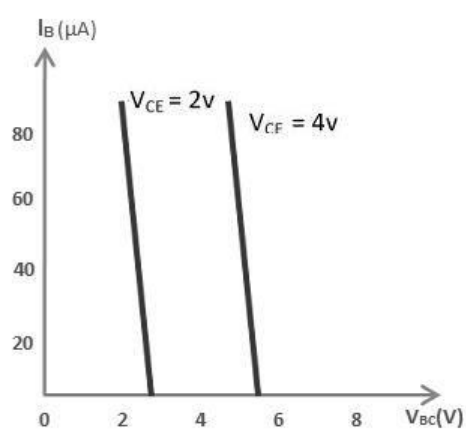
PIN DIAGRAM OF BC107



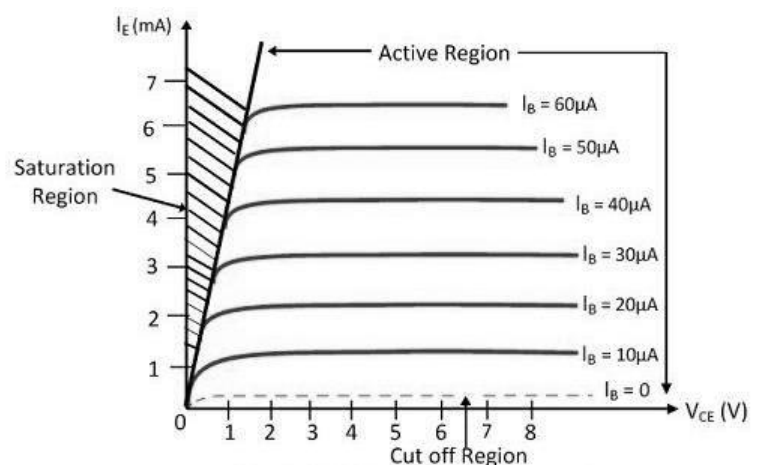
CIRCUIT DIAGRAM: COMMON COLLECTOR CIRCUIT CHARACTERISTICS



MODEL GRAPH:



Input Characteristic Curve



Output Characteristic Curve

Ex. No.: 3(b)

**CHARACTERISTICS OF NPN TRANSISTOR UNDER COMMON
COLLECTOR CONFIGURATION**

AIM:

To plot the Input and Output characteristics of a transistor connected in Common Collector Configuration and to find the dynamic resistance and amplification factor.

APPARATUS REQUIRED:

Sl. No	Components / Equipments	Specifications	Quantity
1	Transistor BC107	Max Rating : 50V 1A, 3W	1
2	Resistors	1k Ω , (or) 470 Ω	2
3	Dual Regulated Power Supply	(0-30)V	1
4	Voltmeters	MC (0-10)V	2
5	Ammeters	MC (0-100) μ A, (0-25)mA	Each One
6	Bread Board		1
7	Connecting Wires		Few

THEORY:

A Bipolar Junction Transistor or BJT is a three terminal device having two PN-junctions connected together in series. Each terminal is given a name to identify it and these are known as the Emitter (E), Base (B) and Collector (C). There are two basic types of bipolar transistor construction, NPN and PNP, which basically describes the physical arrangement of the P-type and N-type semiconductor materials from which they are made. Bipolar Transistors are "CURRENT" Amplifying or current regulating devices that control the amount of current flowing through them in proportion to the amount of biasing current applied to their base terminal. The principle of operation of the two transistors types NPN and PNP, is exactly the same the only difference being in the biasing (base current) and the polarity of the power supply for each type. In CC configuration, Collector is common to both the input and output as shown in figure. The direction of the arrow in the symbol shows current flow between the base and emitter terminal, pointing from the positive P-type region to the negative N-type region, exactly the same as for the standard diode symbol. For normal operation, the emitter-base junction is forward-biased and the collector-base junction is reverse-biased.

TABULATION:

INPUT CHARACTERISTICS:

$V_{CE} =$		$V_{CE} =$	
$V_{BC}(V)$	$I_B (\mu A)$	$V_{BC}(V)$	$I_B (\mu A)$

OUTPUT CHARACTERISTICS:

$I_B =$		$I_B =$	
$V_{CE} (V)$	$I_E (mA)$	$V_{CE} (V)$	$I_E (mA)$

DESCRIPTION:

Input Characteristics: The variation of the base current I_B with the base-collector voltage V_{BC} keeping the collector-emitter voltage V_{CE} fixed, gives the input characteristic in CC mode.

Input Dynamic Resistance (r_i): This is defined as the ratio of change in base collector voltage (ΔV_{BC}) to the resulting change in base current (ΔI_B) at constant collector-emitter voltage (V_{CE}). This is dynamic and it can be seen from the input characteristic, its value varies with the operating current in the transistor:

$$r_i = \left. \frac{\Delta V_{BC}}{\Delta I_B} \right|_{V_{CE}}$$

The value of r_i can be anything from a few hundreds ohms to a few hundred kilo (750K Ω) ohms.

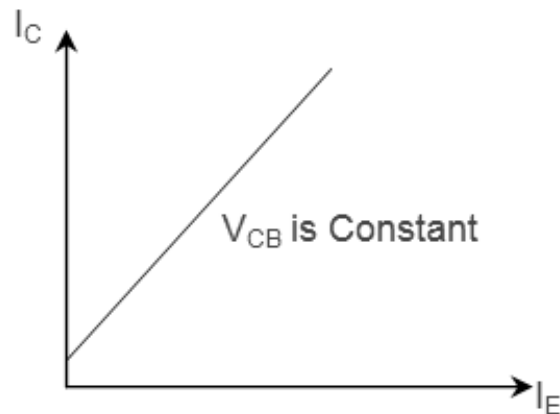
Output Characteristics: The variation of the emitter current I_E with the collector-emitter voltage V_{CE} is called the output characteristic. The plot of I_E versus V_{CE} for different fixed values of I_B gives one output characteristic. Since the emitter current changes with the base current, there will be different output characteristics corresponding to different values of I_B .

Output Dynamic Resistance (r_o): This is defined as the ratio of change in collector-emitter voltage (ΔV_{CE}) to the change in emitter current (ΔI_E) at a constant base current I_B .

$$r_o = \left. \frac{\Delta V_{CE}}{\Delta I_E} \right|_{I_B}$$

The output resistance of the common collector is very low in the order of 50 Ω . This circuit arrangement is mainly used for impedance matching.

Transfer Characteristics: The transfer characteristics are plotted between the input and output currents (I_B versus I_E). Both I_B and I_E increase proportionately.



Current amplification factor (γ)

The current amplification factor is defined as the ratio of change in output current or emitter current I_E to the change in input current or base current I_B . It is expressed by the γ .

$$\gamma_{ac} = \left. \frac{\Delta I_E}{\Delta I_B} \right|_{V_{CE}}$$

The current gain of a common collector amplifier is high. The ratio of I_E and I_B we get what is called dc of the transistor. Hence,

$$\gamma_{dc} = \left. \frac{I_E}{I_B} \right|_{V_{CE}}$$

PROCEDURE:**INPUT CHARACTERISTICS:**

1. Connect the circuit as per the circuit diagram.
2. Set V_{CE} , vary V_{BC} in regular interval of steps and note down the corresponding I_B reading. Repeat the above procedure for different values of V_{BC} .
3. Plot the graph: V_{BC} vs. I_B for a constant V_{CE} .

OUTPUT CHARACTERISTICS:

1. Connect the circuit as per the circuit diagram.
2. Set I_B , Vary V_{CE} in regular interval of steps and note down the corresponding I_E reading. Repeat the above procedure for different values of I_B .
3. Plot the graph: V_{CE} vs. I_E for a constant I_B .

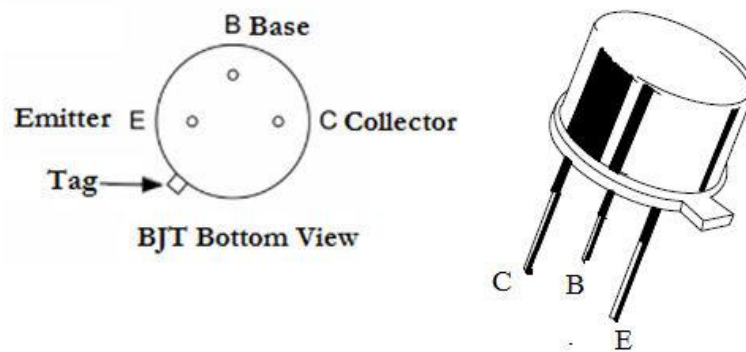
REVIEW QUESTIONS:

1. What are the various configurations of NPN transistor?
2. Why collector of a transistor is the largest region?
3. What is meant by thermal run away?
4. Why amplifier is known as emitter follower?
5. Mention the applications of CC amplifier.
6. What are the differences between CE, CB and CC amplifier?
7. Mention the characteristics of CC amplifier.
8. What is gain BW product?
9. Can we use CC configuration as an amplifier?
10. What is the need for analyzing the transistor circuits using different parameters?
11. What is the significance of hybrid model of a transistor?
12. Is there any phase shift between input and output in CC configuration?
13. Compare the voltage gain and input and output impedances of CE and CC configurations.
14. Which BJT configuration is suitable for impedance matching application? Why?
15. What is the use of heat sink?

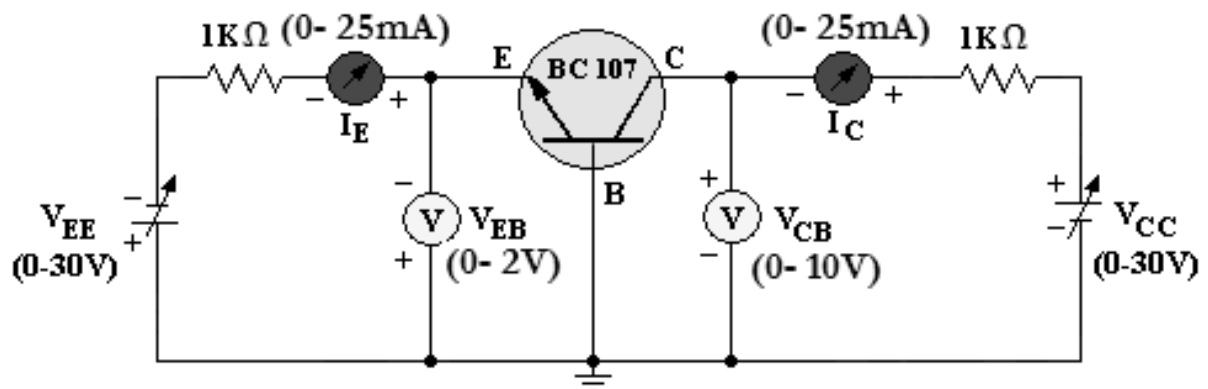
RESULT:

Thus the input and output characteristic of BJT in Common Collector configuration were plotted and the dynamic resistance and amplification factor were obtained.

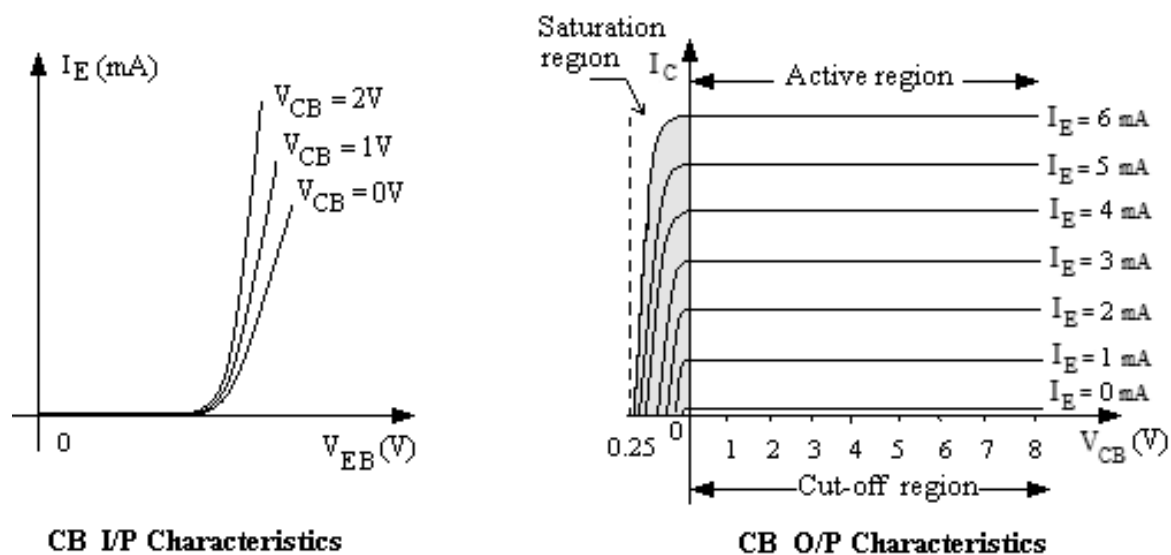
PIN DIAGRAM OF BC107



CIRCUIT DIAGRAM: COMMON BASE CIRCUIT CHARACTERISTICS



MODEL GRAPH:



Ex. No.: 3(c)

CHARACTERISTICS OF NPN TRANSISTOR UNDER COMMON BASE CONFIGURATION

AIM:

To plot the Input and Output characteristics of a transistor connected in Common Base Configuration and to find the dynamic resistance and amplification factor.

APPARATUS REQUIRED:

Sl. No	Components / Equipments	Specifications	Quantity
1	Transistor BC107	Max Rating : 50V 1A, 3W	1
2	Resistors	1k Ω , (or) 470 Ω	2
3	Dual Regulated Power Supply	(0-30)V	1
4	Voltmeters	MC (0-2)V, (0-10)V	Each One
5	Ammeters	MC (0-25)mA	2
6	Bread Board		1
7	Connecting Wires		Few

THEORY:

A Bipolar Junction Transistor or BJT is a three terminal device having two PN-junctions connected together in series. Each terminal is given a name to identify it and these are known as the Emitter (E), Base (B) and Collector (C). There are two basic types of bipolar transistor construction, NPN and PNP, which basically describes the physical arrangement of the P-type and N-type semiconductor materials from which they are made. Bipolar Transistors are "CURRENT" Amplifying or current regulating devices that control the amount of current flowing through them in proportion to the amount of biasing current applied to their base terminal. The principle of operation of the two transistors types NPN and PNP, is exactly the same the only difference being in the biasing (base current) and the polarity of the power supply for each type. In CB configuration, base is common to both the emitter and collector terminal. The direction of the arrow in the symbol shows current flow between the base and emitter terminal, pointing from the positive P-type region to the negative N-type region, exactly the same as for the standard diode symbol. For normal operation, the emitter-base junction is forward-biased and the collector-base junction is reverse-biased.

TABULATION:

INPUT CHARACTERISTICS:

$V_{CB} = 1V$		$V_{CB} = 2V$	
$V_{EB} (V)$	$I_E (mA)$	$V_{EB} (V)$	$I_E (mA)$

OUTPUT CHARACTERISTICS:

$I_E = 1mA$		$I_E = 2mA$	
$V_{BE} (V)$	$I_C (mA)$	$V_{BE} (V)$	$I_C (mA)$

DESCRIPTION:

Input Characteristics: Voltage across Base Emitter junction V_{BE} vs I_E , where V_{CB} constant.

Input Dynamic Resistance (r_i) this is defined as the ratio of change in base emitter voltage (ΔV_{EB}) to the resulting change in emitter current (ΔI_E) at constant collector-emitter voltage (V_{CB}). This is dynamic as its value varies with the operating current in the transistor.

$$r_i = \left. \frac{\Delta V_{EB}}{\Delta I_E} \right|_{V_{CB}}$$

Output characteristics: Voltage across Collector Emitter junction V_{BC} vs I_C where I_E constant

Output Dynamic Resistance (r_o): This is defined as the ratio of change in collector-base voltage (ΔV_{CB}) to the change in collector current (ΔI_C) at a constant base current I_E .

$$r_o = \left. \frac{\Delta V_{CB}}{\Delta I_C} \right|_{I_E}$$

Transfer Characteristics: The transfer characteristics are plotted between the input and output currents (I_E versus I_C).

Current amplification factor (α)

This is defined as the ratio of the change in collector current to the change in emitter current at a constant collector-base voltage (V_{CB}) when the transistor is in active state.

$$\alpha_{ac} = \left. \frac{\Delta I_C}{\Delta I_E} \right|_{V_{CB}}$$

This is also known as small signal current gain and its value is very large. The ratio of I_C and

I_E is called dc of the transistor. Hence,

$$\alpha_{dc} = \left. \frac{I_C}{I_E} \right|_{V_{CB}}$$

Since I_C increases with I_E almost linearly, the values of both dc and ac are nearly equal.

PROCEDURE:**TO FIND THE INPUT CHARACTERISTICS:**

1. Connect the circuit as in the circuit diagram.
2. Keep V_{EE} and V_{CC} in zero volts before giving the supply
3. Set $V_{CB} = 1$ volt by varying V_{CC} . and vary the V_{EE} smoothly with fine control such that emitter current I_E varies in steps of 0.2mA from zero up to 25mA, and note down the corresponding voltage V_{EB} for each step in the tabular form.
4. Repeat the experiment for $V_{CB} = 2$ volts and 3 volts.
5. Draw a graph between V_{EB} vs. I_E against $V_{CB} = \text{Constant}$.

TO FIND THE OUTPUT CHARACTERISTICS:

1. Start V_{EE} and V_{CC} from zero Volts.
2. Set the $I_E = 1\text{mA}$ by using V_{EE} such that, V_{CB} changes in steps of 1.0 volts from zero up to 20 volts, note down the corresponding collector current I_C for each step in the tabular form.
3. Repeat the experiment for $I_E = 3\text{mA}$ and $I_E = 5\text{mA}$, tabulate the readings.
4. Draw a graph between V_{CB} Vs I_C against $I_E = \text{Constant}$.

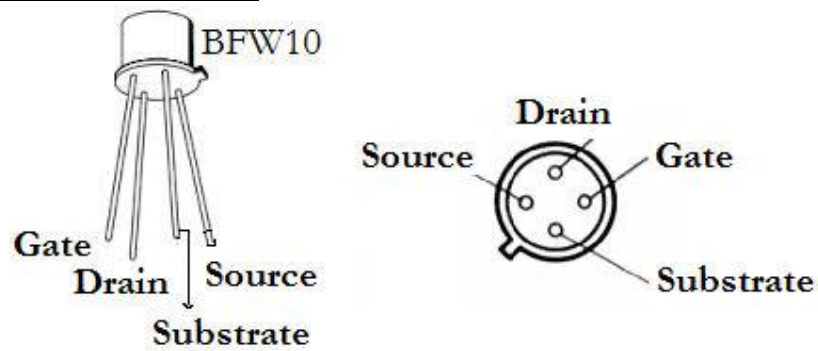
REVIEW QUESTIONS:

1. Give the relation of Ebers moll equation.
2. In a bipolar transistor which region is wider and which region is thinner? Why?
3. State the relation between α and β of a transistor?
4. Express I_c in terms I_{CE0} and I_{CB0} .
5. What does arrow in the transistor symbol indicate?
6. Why emitter of a transistor is highly doped?
7. Which configuration is good as a constant current source? Why?
8. Why α is less than unity?
9. Input and output impedance equations for CB configuration?
10. What is the importance of Fermi level?

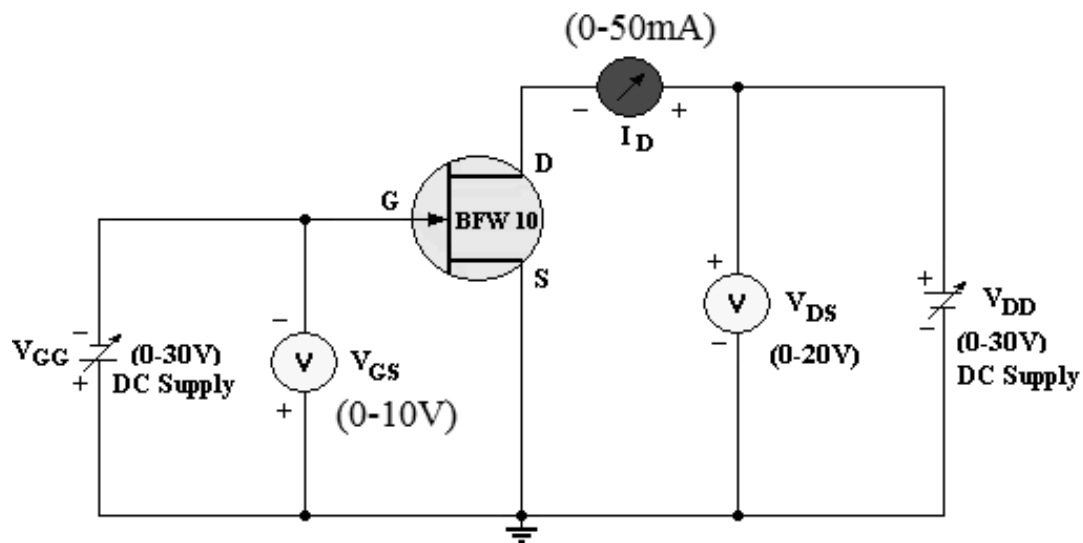
RESULT:

Thus the input and output characteristic of BJT in Common Base configuration were plotted and dynamic resistance and amplification factor were obtained.

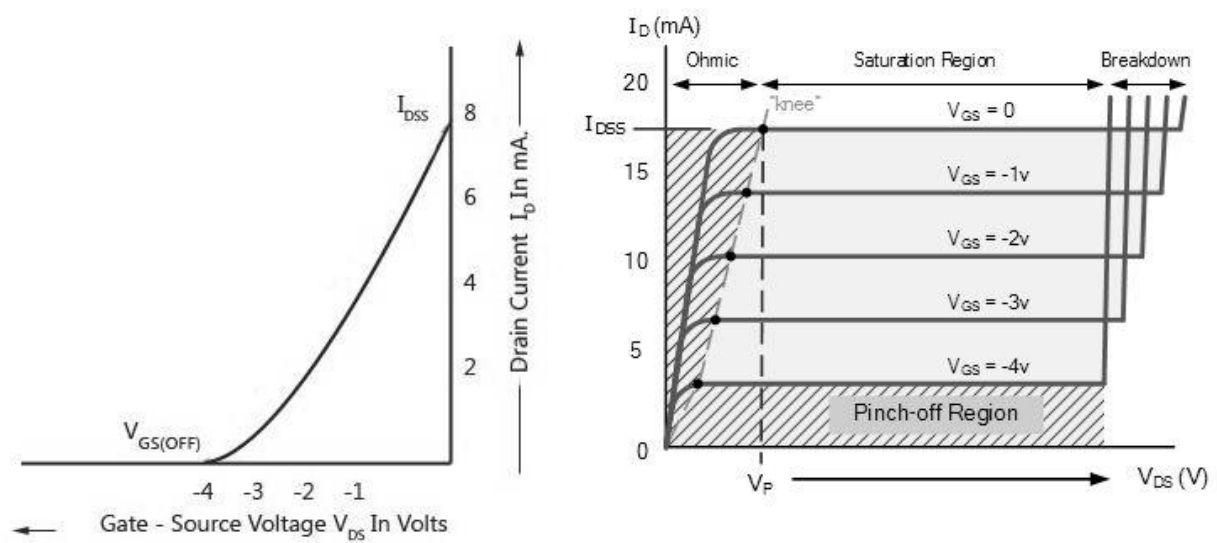
PIN DIAGRAM OF BFW10



CIRCUIT DIAGRAM



MODEL GRAPH:



Ex. No.: 4

CHARACTERISTICS OF JFET AND ITS EQUIVALENT CIRCUIT

AIM:

To plot the Drain and Transfer characteristics of JFET and to find Drain resistance, Transconductance, Amplification factor, Drain saturation current I_{DSS} and Pinch off voltage.

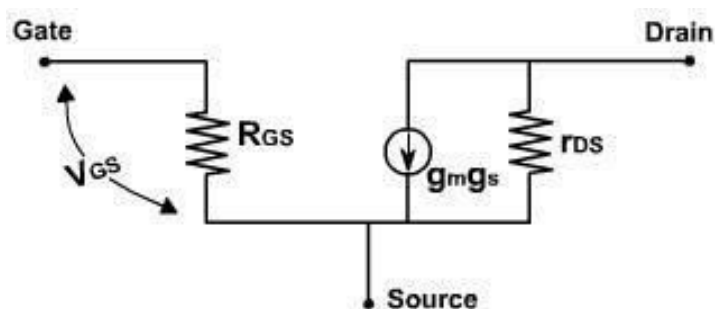
APPARATUS REQUIRED:

Sl. No	Components / Equipments	Specifications	Quantity
1	FET	BFW10 or 11 $I_{DSS} > 8 \text{ mA}$, $V_p < 8 \text{ V}$	1
2	Dual Regulated Power Supply	(0-30)V	1
3	Voltmeters	MC (0-10)V, MC (0-20)V	Each One
4	Ammeters	MC (0-50) mA	1
5	Bread Board		1
6	Connecting Wires		Few

THEORY:

The Field Effect Transistor (FET) is a three terminal device. Three terminals are Drain (D), Source (S), Gate (G) and fourth terminal is substrate/body/shield/Bulk but it is not used. In FET, current flow is due to only one type of charge particles, either electrons or holes. So FET is known as unipolar device. The name “field effect” is derived from the fact that the current is controlled by an electric field set up in the device by an externally applied voltage. Thus FET is a voltage controlled device while bipolar transistor is current controlled device.

JFET AC Equivalent Circuit:



TABULAR COLUMN:

Drain characteristics

[illegible]

Transfer characteristics

[illegible]

PROCEDURE:

DRAIN CHARACTERISTICS:

1. Connect the circuit as per the circuit diagram and start with VGG and VDD keeping at zero volts.
2. Keep VGG such that $V_{GS} = 0$ volts, Now vary VDD such that V_{DS} Varies in steps of 1 volt up to 10 volts. And Note down the corresponding Drain current I_D .
3. Repeat the above experiment with $V_{GS} = -2V$ and $-4V$ and tabulate the readings.
4. Draw a graph V_{DS} Vs I_D against V_{GS} as parameter on graph.
5. From the above graph calculate r_d and note down the corresponding diode current against the voltage in the tabular form.
6. Draw the graph between voltages across the Diode vs. Current through the diode in the first quadrant as shown in model graph.

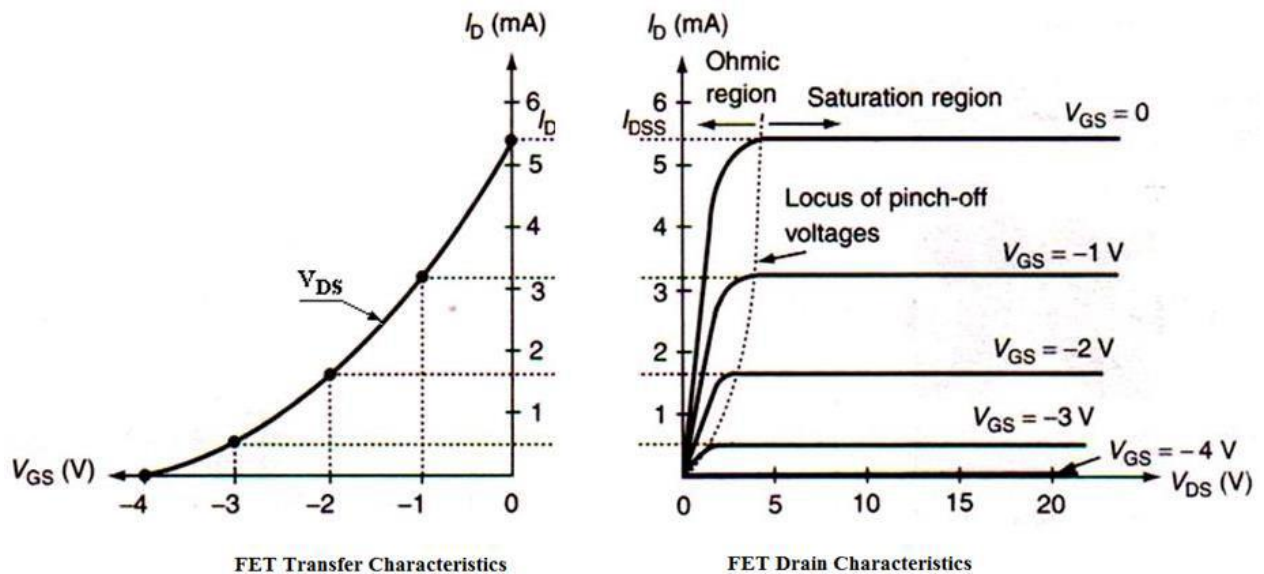
TRANSFER CHARACTERISTICS:

1. Set VGG and VDD at zero volts .keep $V_{DS} = 2V$.
2. Vary VGG such that V_{GS} varies in steps of 0.5 volts. Note down the corresponding
3. Drain current I_D , until $I_D = 0mA$ and Tabulate the readings.
4. Repeat the above experiment for $V_{DS} = 4$ Volts and 6 Volts and tabulate the readings.
5. Draw graph between V_{GS} Vs I_D with V_{DS} as parameter.
6. From the graph find g_m .

PRECAUTIONS:

1. Check the wires for continuity before use.
2. Keep the power supply at zero volts before starting the experiment.
3. All the contacts must be intact.
4. For a good JFET I_D will be ≥ 11.0 mA at $V_{GS} = 0.0$ volts if not change the JFET.
5. Make sure while selecting the source, drain and gate terminals of the FET.

MODEL GRAPH:



CALCULATIONS:

Calculation of r_d :

Construct a Triangle on one of the output characteristic for a particular V_{GS} in the active region and find ΔV_{DS} and ΔI_D .

Drain resistance **r_d** = $\Delta V_{DS} / \Delta I_D$ (V_{GS} = constant)

Calculation of g_m :

Construct a Triangle on one of the Transfer characteristics for a particular V_{DS} find ΔV_{GS} and ΔI_D .

Transconductance **g_m** = $\Delta I_D / \Delta V_{GS}$ (V_{DS} = constant).

Calculation of μ :

Amplification factor **μ** = $g_m \times r_d$.

REVIEW QUESTIONS:

1. Why it is called by name “Field Effect Transistor”?
2. What are the advantage of FET over BJT?
3. What are the disadvantages of FET?
4. What is the significance of arrowhead in FET symbol?
5. Why FET is called unipolar device?
6. Define VVR.
7. What are the applications of FET?
8. Why FET is called us voltage controlled device?
9. What are the characteristics of JFET?
10. Why input resistance in FET amplifier is more than the BJT amplifier?
11. What is pinch off voltage?
12. What is Enhancement mode and Depletion mode?
13. Draw the Equivalent circuit of JFET for low frequencies.
14. Write the mathematical equation for g_m in terms of g_{mo} .
15. Write equation of FET I_D in terms of V_{GS} and V_p .

RESULT:

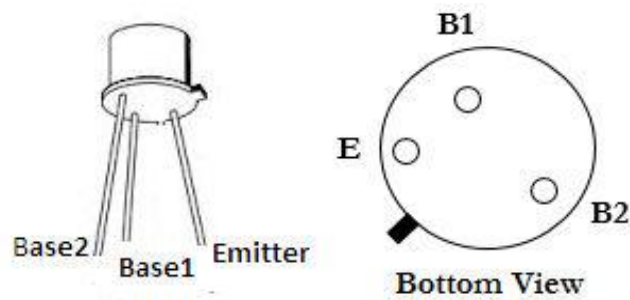
Thus the drain and transfer characteristic of JFET is drawn and following parameters are observed.

Drain resistance (r_d) =

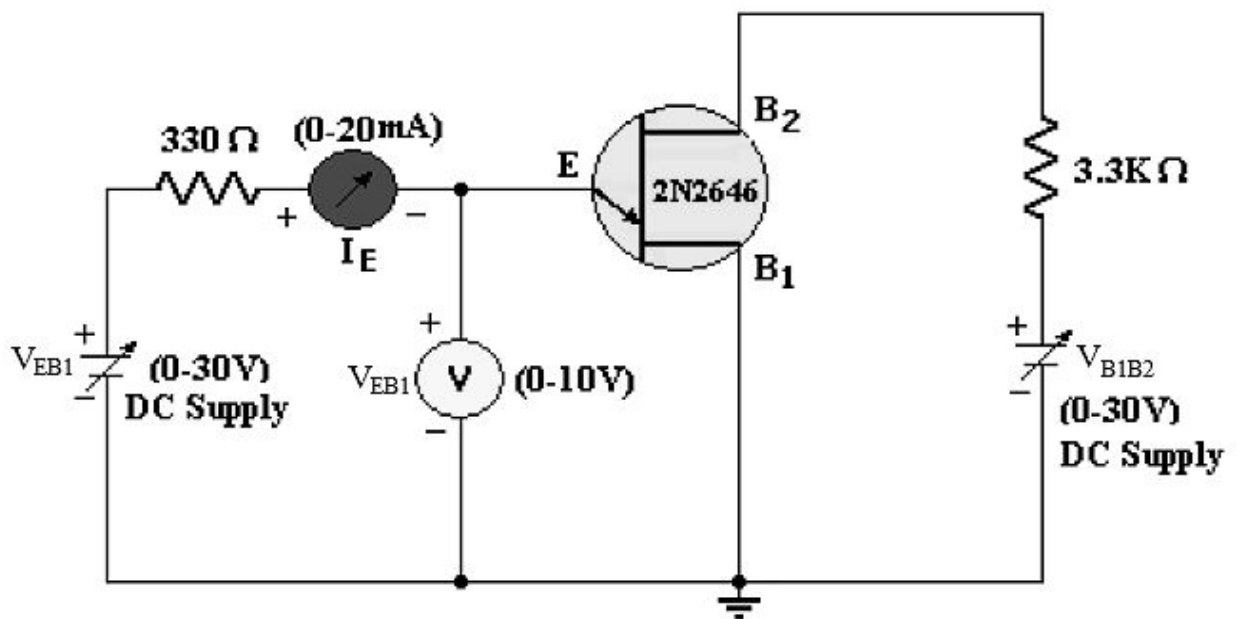
Trans conductance (g_m) =

Amplification factor (μ) =

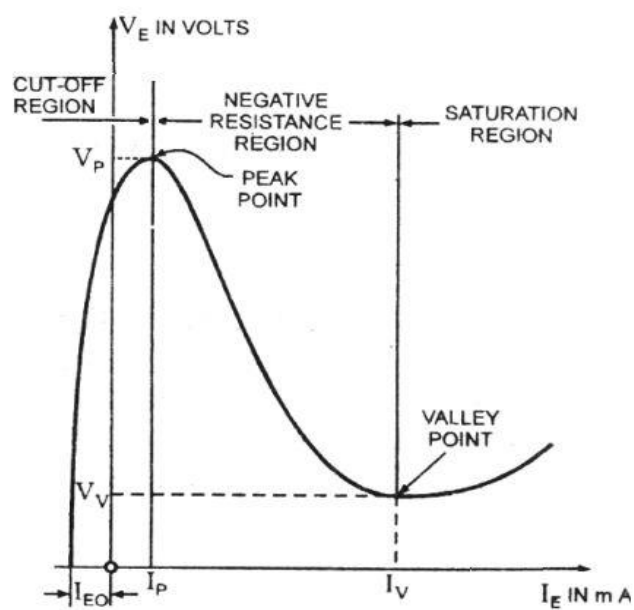
PIN DIAGRAM



CIRCUIT DIAGRAM:



MODEL GRAPH



Ex. No.: 5

CHARACTERISTICS OF UJT AND GENERATION OF SAWTOOTH WAVEFORM

AIM:

To plot VI Characteristics and generate sawtooth waveform using UJT.

APPARATUS REQUIRED:

Sl. No	Components / Equipments	Specifications	Quantity
1	UJT	2N2646	1
2	Resistors	330 Ω , 3.3k Ω	Each One
3	Dual Regulated Power Supply	(0-30)V	1
4	Voltmeters	MC (0-10)V	1
5	Ammeters	MC (0-25) mA	1
6	Bread Board		1
7	Connecting Wires		Few

THEORY:

Unijunction transistor is a negative resistance silicon controlled device. UJT has three terminals emitter (E), base1 (B1) & base2 (B2). The UJT finds its main application in switching circuits and in relaxation oscillators. It consists of an n-type Si semiconductor bar, which is lightly doped connected between two ohmic contacts B1 and B2. A heavily doped P-region is diffused into the n-type bar forming a pn junction in the middle of the base bar. A terminal is taken out of this region & named as emitter. The emitter is always forward biased with respect to the base 1 and base 2 is kept at a higher +ve potential with respect to base 1.

INTRINSIC STAND-OFF RATIO:

We know that, from the equivalent circuit,

$$V_{B1} = V_{BB} \cdot \frac{R_{b1}}{R_{b1} + R_{b2}} = \eta V_{BB}$$

The diode firing takes place when $V_E > (V_{B1} + V_D)$

Where V_D is voltage drop across diode. The emitter firing potential is given by,

$$V_P = \eta V_{BB} + V_D$$

where V_D is 0.7V

$$\eta = \frac{R_{b2} - V_D}{V_{BB}}$$

TABULATION:

$V_{B1B2} = 2V$		$V_{B1B2} = 4V$		$V_{B1B2} = 6V$	
V_{EB1} (v)	I_E (mA)	V_{EB1} (v)	I_E (mA)	V_{EB1} (v)	I_E (mA)

Design for sawtooth signal generation:

$$V_C = V_{BB} (1 - e^{-t/R_E C_E})$$

$$V_P = \eta V_{BB} = V_{BB} (1 - e^{-t/R_E C_E})$$

Consider $\eta = 1 - e^{-t/R_E C_E}$

$$e^{-t/R_E} C_E = 1 - \eta$$

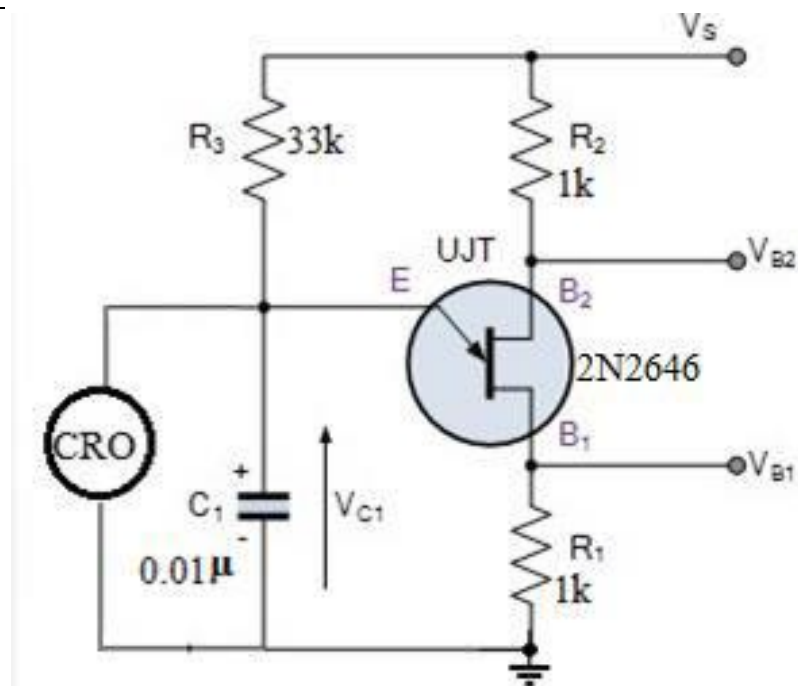
$$t = R_E C_E \log_e(1 / (1 - \eta))$$

$$t = 2.303 R_E C_E \log_{10} (1 / (1 - \eta))$$

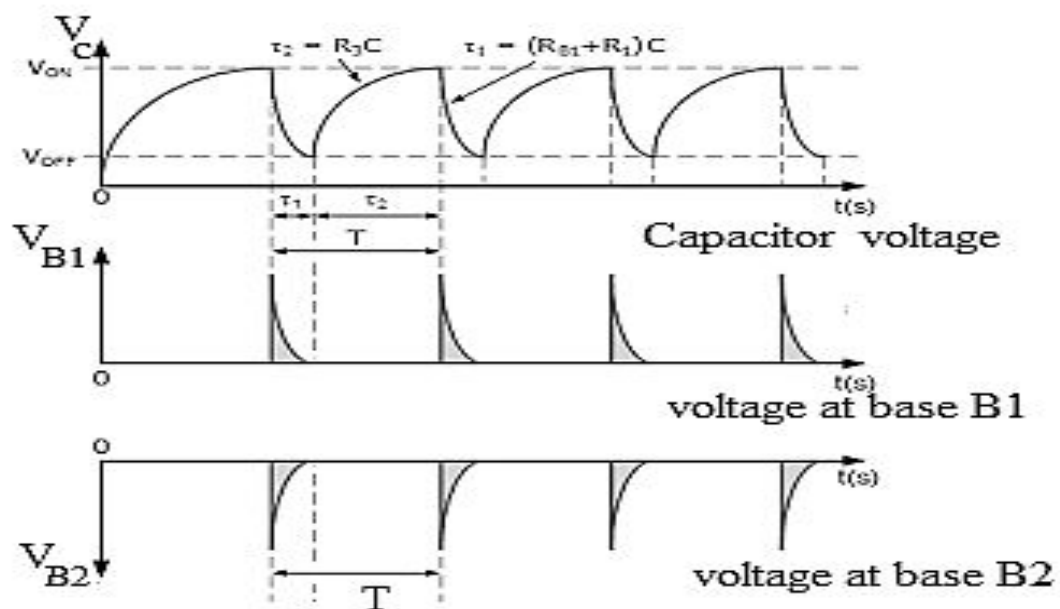
PROCEDURE:

1. Connections are given as per the circuit diagram.
2. The voltage across B1 and B2 (V_{B1B2}) is kept constant (say 5V), emitter voltage V_{B1E} is varied in steps & the corresponding I_E values are tabulated.
3. The above procedure is repeated for $V_{B1B2}=10V$.
4. Graph is plotted between V_{B1E} and I_E for a constant value of V_{B1B2} .
5. From the graph, peak voltage & valley voltage is obtained.

CIRCUIT DIAGRAM FOR SAWTOOTH WAVEFORM GENERATION USING UJT



MODEL GRAPH:



REVIEW QUESTIONS:

1. What are the applications of UJT?
2. What are other names for UJT?
3. What is intrinsic standoff ratio?
4. Define valley voltage & peak voltage.
5. Differentiate BJT and UJT.
6. What does UJT stands for? Justify the name UJT.
7. What is the difference between UJT & FET?
8. Why does negative resistance region appears in UJT?
9. What is inter-base resistance?
10. What is relaxation oscillator?

RESULT:

Thus the static emitter characteristics of UJT drawn & the following values were determined and sawtooth waveform also generated.

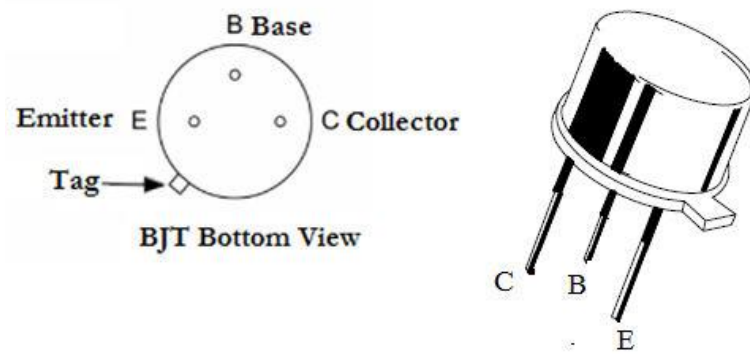
Peak voltage =

Valley voltage =

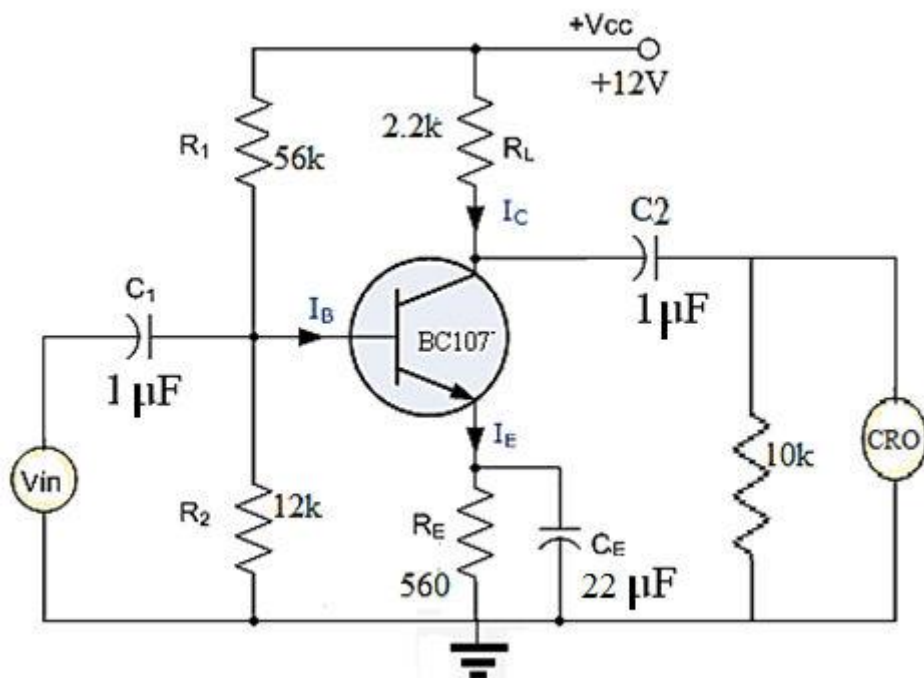
Intrinsic standoff ratio =

Time period of the sawtooth waveform=

PIN DIAGRAM:



CIRCUIT DIAGRAM FOR CE AMPLIFIER:



Ex. No.: 6

**DESIGN AND FREQUENCY RESPONSE CHARACTERISTICS
OF A COMMON EMITTER AMPLIFIER**

AIM:

To design and construct BJT CE Amplifier using voltage divider bias and to obtain its frequency response.

APPARATUS REQUIRED:

Sl. No	Components / Equipments	Specifications	Quantity
1	Transistor BC107	Max Rating : 50V 1A, 3W	1
2	Resistors	56k Ω , 12k Ω , 2.2k Ω , 10k Ω , 560 Ω	Each One
3	Capacitor	0.1 μ F, 22 μ F	2,1
4	Dual Regulated Power Supply	(0-30)V	1
5	CRO	(0-30)MHz	1
6	Function Generator	(0 – 1)MHz	1
7	Bread Board		1
8	Connecting Wires		Few
9	BNC CRO Probe		2

THEORY:

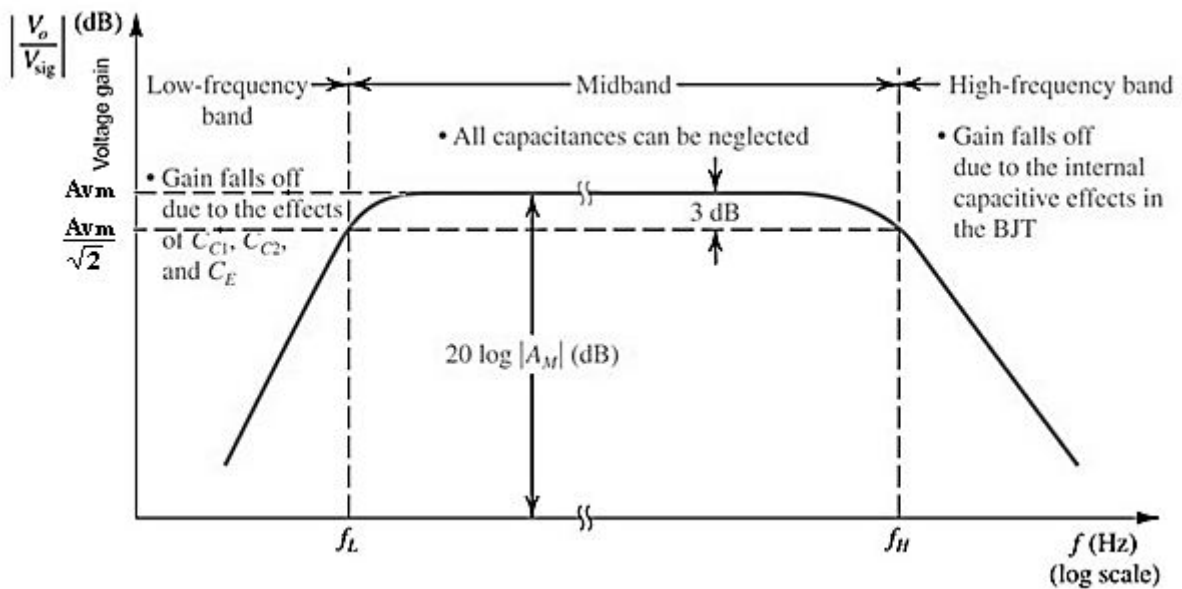
Common Emitter amplifier has the emitter terminal as the common terminal between input and output terminals. The emitter base junction is forward biased and collector base junction is reverse biased, so that transistor remains in active region throughout the operation. When a sinusoidal AC signal is applied at input terminals of circuit during positive half cycle the forward bias of base emitter junction V_{BE} is increased resulting in an increase in I_B , The collector current I_c is increased by β times the increase in I_B , V_{CE} is correspondingly decreased. i.e. output voltage gets decreased. Thus in a CE amplifier a positive going signal is converted into a negative going output signal i.e. 180° phase shift is introduced between output and input signal and it is an amplified version of input signal.

TABULATION:

$$V_i = 1V$$

Frequency (Hz)	V _o (V)	Gain= 20log(V _o /V _i)dB

MODEL GRAPH:



DESIGN:

$$V_{CC} = 12 \text{ V}, I_C = 2 \text{ mA}, R_B = 10 \text{ k}\Omega, h_{fe} = 100, h_{ie} = 2 \text{ k}\Omega$$

$$V_{CE} = V_{CC} / 2 = 12 / 2 = 6 \text{ V}$$

$$V_E = V_{CC} / 10 = 12 / 10 = 1.2 \text{ V}$$

$$I_E \approx I_C = 2 \text{ mA}$$

$$R_E = V_E / I_E = 1.2 \text{ V} / 2 \text{ mA} = 600 \Omega$$

$$\text{Choose, } R_E = 560 \Omega$$

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E$$

$$R_C = (V_{CC} - V_{CE} - I_E R_E) / I_C$$

$$R_C = (12 - 6 - 1.2) / 2 \text{ mA}$$

$$R_C = 2.4 \text{ k}\Omega$$

$$\text{Choose, } R_C = 2.7 \text{ k}\Omega$$

$$V_{BE} = V_B - V_E$$

$$V_B = V_{BE} + V_E$$

$$V_B = 0.7 + 1.2 = 1.9 \text{ V}$$

$$V_B = V_{CC} (R_2 / (R_1 + R_2)) = 1.9 \text{ V}$$

$$R_2 / (R_1 + R_2) = 1.9 \text{ V} / 12 \text{ V} = 0.158$$

$$R_B = 10 \text{ k} = R_1 R_2 / (R_1 + R_2) = R_1 (0.158)$$

$$R_1 = 63.157 \text{ k}\Omega$$

$$R_2 / (R_1 + R_2) = 0.158 \Rightarrow R_2 = 11.58 \text{ k}\Omega$$

$$\text{Choose, } R_1 = 56 \text{ k}\Omega \text{ and } R_2 = 12 \text{ k}\Omega$$

$$X_E = R_E / 10 = 600 / 10 = 60 \Omega$$

$$C_E = 1 / (2\pi f X_E) = 26.5 \mu\text{F} \quad (\text{for } f = 1 \text{ kHz}),$$

$$\text{Choose Coupling capacitors } C_1 = C_2 = 1 \mu\text{F}$$

PROCEDURE:

1. Connect the circuit as per the circuit diagram
2. Set $V_{in} = 2V$ in the signal generator. Keeping input voltage constant, vary the frequency from 1Hz to 3MHz in regular steps.
3. Note down the corresponding output voltage.
4. Plot the graph: Gain in dB Vs Frequency in Hz.
5. Calculate the Bandwidth from the Frequency response graph.

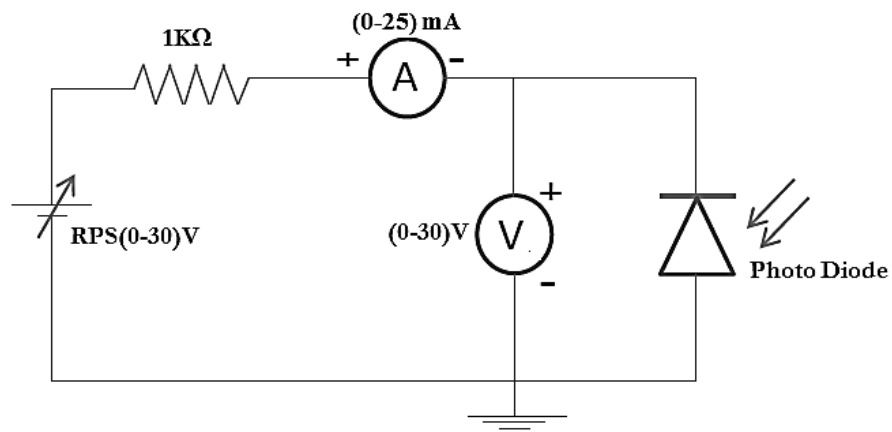
REVIEW QUESTIONS:

1. What are the operating modes of BJT with reference to junction biasing?
2. Why CE configuration is preferred over CB configuration?
3. Write some applications of CE amplifier.
4. What will be the input and output impedance of CE amplifier?
5. What is the voltage and current gain of CE amplifier?

RESULT:

Thus a BJT CE Amplifier with voltage divider bias was designed and plotted the frequency response curve.

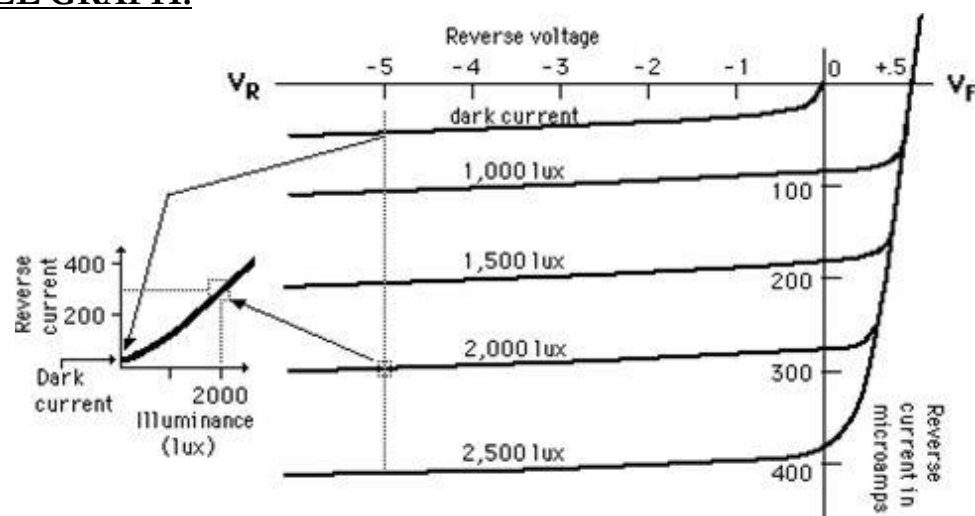
CIRCUIT DIAGRAM:



TABULATION:

Reverse voltage (V)	Reverse current (In darkness) (mA)	Reverse current (In illumination) (mA)

MODEL GRAPH:



Ex. No.: 7(a)

CHARACTERISTICS OF PHOTO DIODE

AIM:

To study the VI characteristics of a Photo Diode.

APPARATUS REQUIRED:

Sl. No	Components / Equipments	Specifications	Quantity
1	Photodiode	-	1
2	Resistors	1k Ω	1
3	Regulated Power Supply	(0-30)V	1
4	Ammeter	(0-25)mA	1
5	Voltmeter	(0-30) V	1
6	Incandescent Lamp	-	1
7	Bread Board		1
8	Connecting Wires		Few

THEORY:

Photo diode is connected in reverse biased condition. The depletion region width is large under normal condition. It carries small reverse current. When light is incident through glass window on PN junction, photons in the light bombards with the PN junction and some energy is imparted to the valence electron. Due to this valence electrons are dislodged from the covalent bonds and become a free electron. Thus total number of minority carriers' increases thereby increasing the reverse current.

PROCEDURE:

1. Switch on the power supply.
2. Photodiode is subjected to darkness and illumination and the following steps are followed each time.
3. By varying the supply voltage in steps of 1V, note down the reverse voltage(V_r) and corresponding reverse current (I_r)
4. Plot the graph between reverse voltage and reverse current.

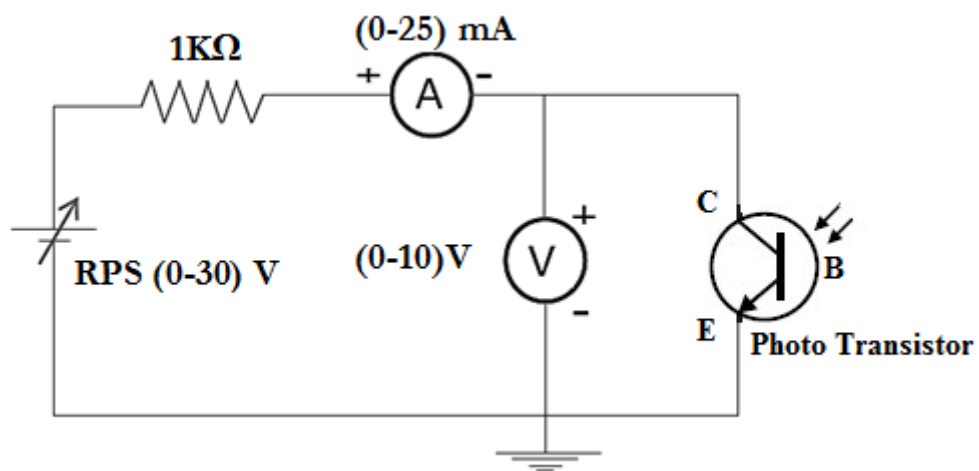
REVIEW QUESTIONS:

1. What is Photo diode?
2. What is the output signal of a Photo diode?
3. What happens if the Photo diode is biased with a voltage larger than the specified maximum reverse bias?
4. What is Photo voltaic effect?
5. Explain the principle of photoconduction.
6. What are the applications of Photo diode?
7. In what sense does the Photo diode differs from a rectifier diode?
8. Why Photo diode works in reverse bias condition only?
9. Differentiate between Photo diode and LED.
10. Between what parameters is the Photo diode characteristics curve plotted?

RESULT:

Thus the VI characteristic of a Photo diode was plotted in the presence and absence of illumination.

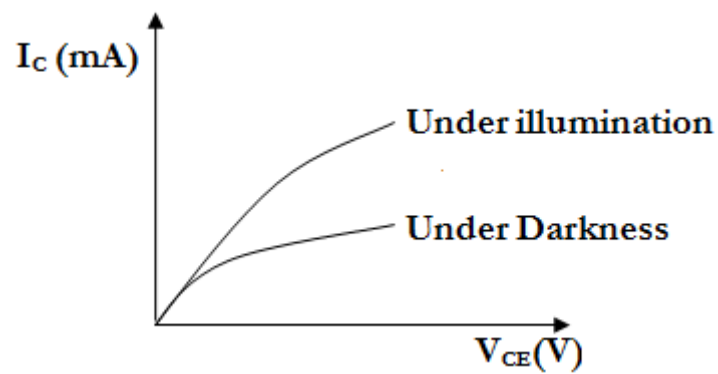
CIRCUIT DIAGRAM:



TABULATION:

S. No	Under Darkness		Under illumination	
	$V_{CE}(V)$	$I_C(mA)$	$V_{CE}(V)$	$I_C(mA)$

MODEL GRAPH:



Ex. No.: 7(b)

CHARACTERISTICS OF PHOTO TRANSISTOR

AIM:

To study the VI characteristics of a Photo Transistor.

APPARATUS REQUIRED:

Sl. No	Components / Equipments	Specifications	Quantity
1	Photo Transistor	-	1
2	Resistors	1k Ω	1
3	Regulated Power Supply	(0-30)V	1
4	Ammeter	(0-25)mA	1
5	Voltmeter	(0-10) V	1
6	Incandescent Lamp	-	1
7	Bread Board		1
8	Connecting Wires		Few

THEORY:

Phototransistor helps us to achieve photo multiplication or photo current enhancement. In phototransistor, pairs are generated on the base region by illumination and some majority carriers diffuse into the emitter, resulting in an injection current which is large. The base load can even be left open but still majority current will cause injection in this structure.

PROCEDURE:

1. Switch on the power supply.
2. Photodiode is subjected to darkness and illumination and the following steps are followed each time.
3. By varying the supply voltage in steps of 1V, note down the voltage(V_{CE}) and corresponding current (I_c)
4. Plot the graph between voltage and current.

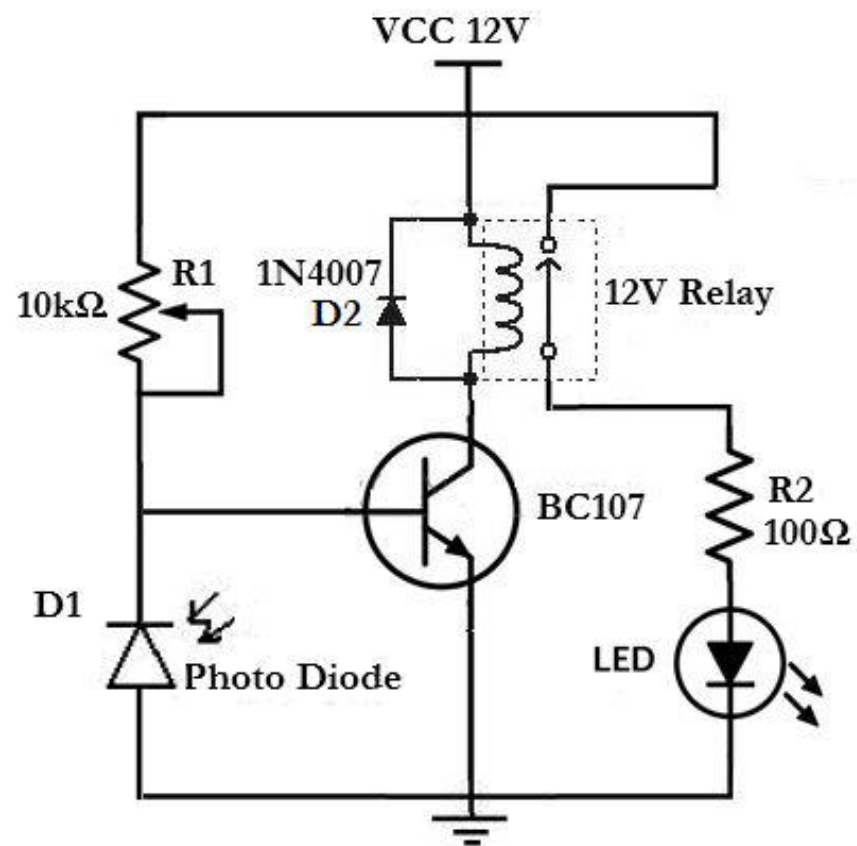
REVIEW QUESTIONS:

1. Explain the operation of a phototransistor.
2. Explain photo multiplication effect.
3. What is a Photo Transistor?
4. What are the applications of Photo transistor?
5. What are the advantages and disadvantages of Photo transistor?
6. In which region does the photo transistor operates?
7. Draw the basic arrangement of biasing of a phototransistor.
8. What is meant by dark resistance in photo transistor?
9. Differentiate between photo diode and phototransistor.
10. Define – Photoluminescence and list the various types of luminescence.

RESULT:

Thus the VI characteristic of a Photo Transistor was plotted in the presence and absence of illumination.

CIRCUIT DIAGRAM:



Ex. No.: 7(c)

STUDY OF LIGHT ACTIVATED RELAY CIRCUIT

AIM:

To study the working principle of Light activated Relay circuit.

APPARATUS REQUIRED:

Sl. No	Components / Equipments	Specifications	Quantity
1	Transistor	BC107	1
2	Photo diode	-	1
3	PN Diode	1N4007	1
4	Resistors	100 Ω	1
5	Regulated Power Supply	(0-30)V	1
6	Decade Resistance Box	-	1
7	Relay	12 V SPST	1
8	LED	Red Color	1
9	Incandescent Lamp	-	1
10	Bread Board		1
11	Connecting Wires		Few

THEORY:

A photo relay or light activated relay is a circuit which opens and closes the relay contacts according to the light. Here a photo diode is used to sense the light. The photo diode offers a high resistance when there is no light falling on it. Here the photo diode is connected in reverse biased condition. The only current flowing through it will be due to the minority carriers. When light falls on it, the current due to the minority carriers increase and the diode offers a low resistance. As a result the voltage across the diode will not be sufficient to make the transistor Q1 forward biased and the relay will OFF. When there is darkness the photo diode resistance increases and the voltage across it will become enough to forward bias the transistor Q1 making the relay ON. The diode D2 is used as a freewheeling diode to protect the transistor from transients produced to the switching of relay. By this way the load connected through the relay contacts can be switched ON and OFF according to the light falling on the photo diode.

PROCEDURE:

1. Assemble the circuit on a Bread board.
2. The circuit can be powered from 12V DC.
3. The preset R1 can be used to adjust the sensitivity of the circuit.
4. The Diode D1 can be any general purpose photo diode.

REVIEW QUESTIONS:

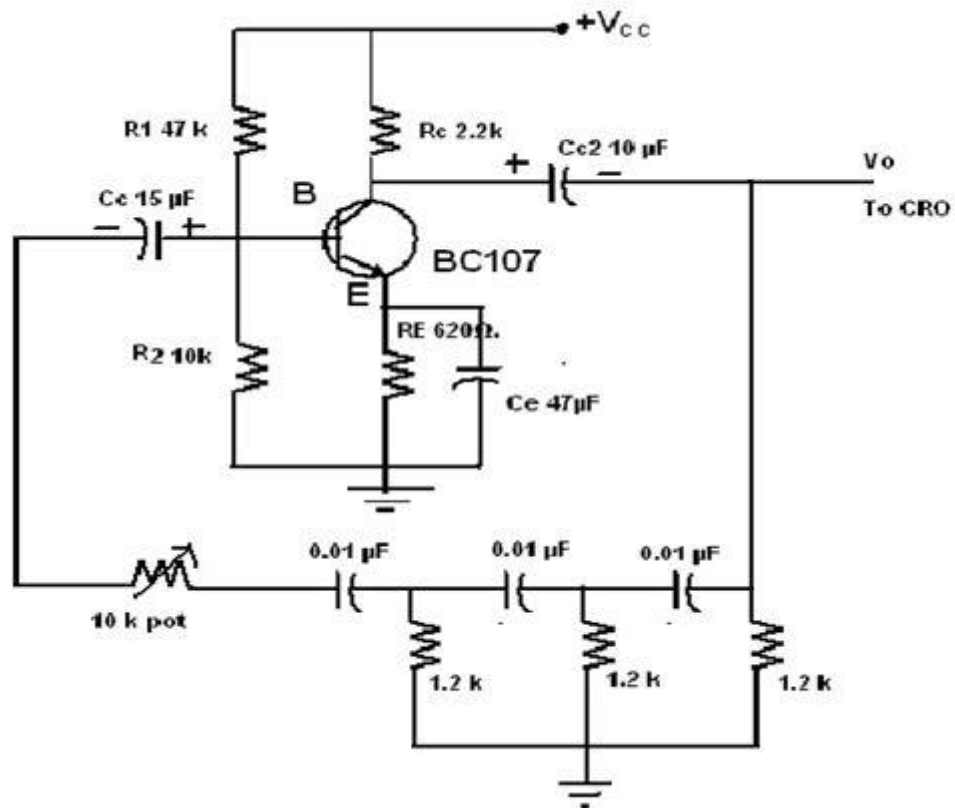
1. What is a light activated relay?
2. Which type of transistor configuration is used in relay circuit?
3. How can the sensitivity of circuit increased?
4. How is the intensity of light related to resistance offered by LDR/Photodiode?
5. What are the various applications of light sensitive circuits?

RESULT:

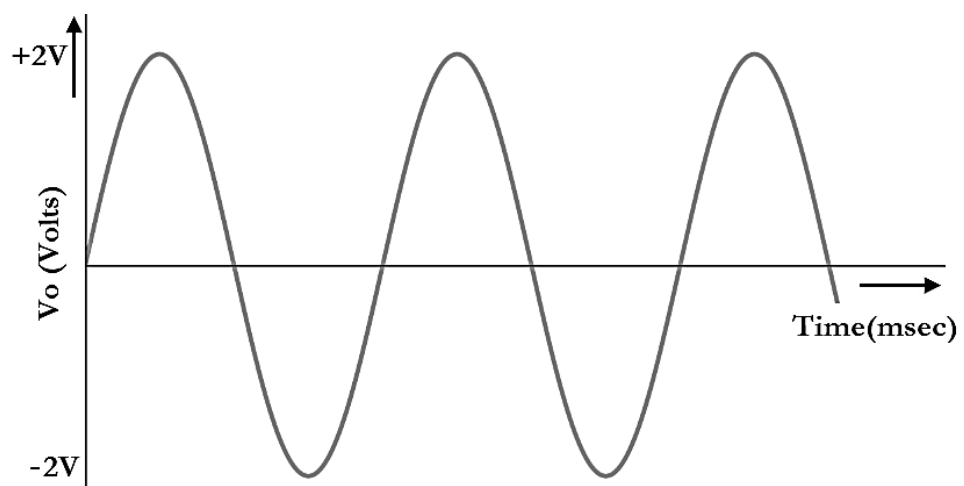
Thus the working of Light activated Relay circuit was studied.

CIRCUIT DIAGRAM

RC PHASE SHIFT OSCILLATOR



MODEL GRAPH



Ex. No.: 8(a)

RC PHASE SHIFT OSCILLATOR

AIM:

To design and construct a RC phase shift oscillator for the given frequency (f_0).

APPARATUS REQUIRED:

Sl. No	Components / Equipments	Specifications	Quantity
1	Transistor	BC107	1
2	Resistors	1.2k Ω , 47k Ω , 10k Ω , 2.2k Ω , 620 Ω	3, 1, 1 1, 1
3	Capacitor	0.01 μ F, 10 μ F, 15 μ F 47 μ F,	3, 1 1, 1
4	CRO	(0 – 30) MHz	1
5	Regulated Power Supply	(0 – 30)V	1
6	Function Generator	(0-1)MHz	1
7	Decade Resistance Box	-	1
8	Bread Board		1
9	Connecting Wires		Few

THEORY:

In the RC phase shift oscillator, the required phase shift of 180° in the feedback loop from the output to input is obtained by using R and C components, instead of tank circuit. Here a common emitter amplifier is used in forward path followed by three sections of RC phase network in the reverse path with the output of the last section being returned to the input of the amplifier. The phase shift Φ is given by each RC section $\Phi = \tan^{-1} (1/\omega RC)$. In practice R-value is adjusted such that Φ becomes 60° . If the value of R and C are chosen such that the given frequency for the phase shift of each RC section is 60° . Therefore at a specific frequency the total phase shift from base to transistor's around circuit and back to base is exactly 360° or 0° . Thus the Barkhausen criterion for oscillation is satisfied.

DESIGN:

$$V_{cc}=12\text{V}, I_c=1\text{mA}, \beta=100, R_E = 560 \, \Omega$$

$$V_{ce}=V_{cc}/2=6\text{V}, \quad V_{re}=0.1V_{cc}=1.2\text{V}$$

$$V_b=V_{re}+0.7=1.9\text{V},$$

$$R_1=V_{cc}/10I_b - R_2$$

$$=12/(10*20\mu\text{A}) - 10 \, \text{K} = 47 \, \text{K} \, \Omega$$

$$R_2=V_b/10I_b = .9/(10*20\mu\text{A})=9.5\text{K} \, \Omega=10 \, \text{K} \, \Omega$$

$$R_c=V_{cc}-V_{ce}- (I_e R_E/I_c)$$

$$=2.4 \, \text{K} \, \Omega = 2.2 \, \text{K} \, \Omega$$

$$\text{Oscillating frequency } f_o=1/(2\pi R C \sqrt{(6+4(R_c/R))})$$

$$\text{For } f_o= 3 \, \text{kHz}$$

$$C = 1/2\pi R f_o \sqrt{(6+4(R_c/R))}$$

$$= 0.012 \, \mu\text{F}$$

$$\text{Consider } C = 0.01 \, \mu\text{F}$$

PROCEDURE:

1. The circuit is constructed as per the given circuit diagram.
2. The supply voltage of +12 volts and ground are given to the constructed circuit.
3. The output sine wave generated from the circuit is verified in the CRO and the theoretical frequency is calculated and verified with the practical frequency.

REVIEW QUESTIONS

1. What is an Oscillator circuit?
2. What are the conditions for sustained oscillator?
3. What are the classifications of Oscillators?
4. What are the advantage and disadvantages of negative feedback?
5. What type of feedback is preferred in oscillators?
6. What is the frequency of oscillation for RC phase shift oscillator?
7. What is the minimum value of h_{fe} for the oscillations in transistorized RC Phase shift oscillator?
8. Why RC oscillators cannot generate high frequency oscillations?
9. What are the applications of RC phase shift oscillators?
10. Why we need a phase shift between input and output signal?

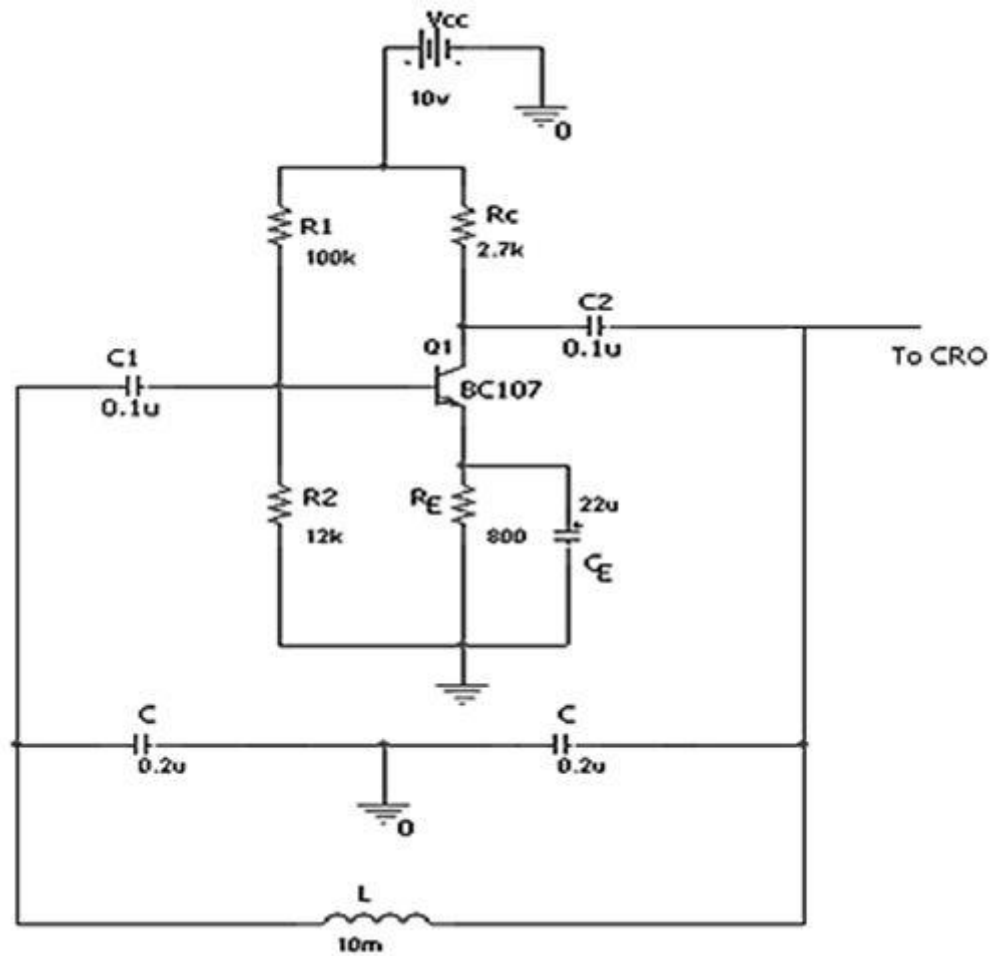
RESULT:

Thus a sine wave with required phase shift is produced using transistor phase shift oscillator. Thus,

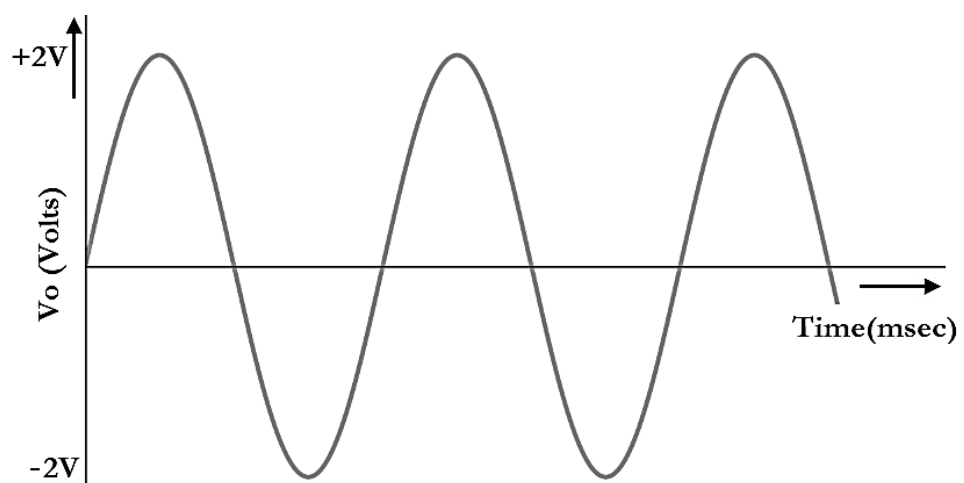
Theoretical Oscillation Frequency = _____

Practical Oscillation Frequency = _____

CIRCUIT DIAGRAM:
COLPITTS OSCILLATOR



MODEL GRAPH:



Ex. No.: 8(b)

COLPITTS OSCILLATOR

AIM :

To design and construct a Hartley and Colpitts oscillator.

COMPONENTS AND EQUIPMENTS REQUIRED:

Sl. No	Components / Equipments	Specifications	Quantity
1	Transistor	BC107	1
2	Resistors	100k Ω , 2.7k Ω , 12k Ω , 800 Ω	Each 1
3	Capacitor	0.1 μ F, 0.2 μ F, 22 μ F	2, 2, 1
4	CRO	(0-30)MHz	2
5	Decade Inductance box	-	1
6	Regulated Power Supply	(0 – 30)V	1
7	Bread Board		1
8	Connecting Wires		Few

THEORY

If gain A of the amplifier is just sufficient to overcome the attenuator β of the β - network. We get sinusoidal oscillations. Mathematically If $A\beta$ is for greater than 1 square wave results in however, if $A\beta$ is less than 1 no oscillations will occur. The Colpitts and Hartley Oscillator is a LC oscillator. Generally, LC oscillators are designed to operate in the radio – frequency range above 1MHz however, they can also be designed to produce oscillations in the low audio – frequency range. But for low frequency operation, the size of the inductors to be used become larger and larger as the frequency becomes smaller and smaller and this puts a limit on the low frequency range of oscillators employing LC – coupling network.

DESIGN:

$$\text{Frequency of oscillation } f_o = \frac{1}{2\pi\sqrt{LC_{eq}}}$$

$$\text{where , } C_{eq} = (C_1C_2)/(C_1+C_2)$$

Let $C_1 = 0.2\mu\text{F}$, $C_2 = 0.2\mu\text{F}$ and $L = 10\text{mH}$

Then , $f_o = 5\text{kHz}$

DESIGN:

$$V_{CC} = 10V, I_C = 1.2mA, R_B = 15k\Omega$$

$$V_E = V_{CC} / 10 = 10V / 10 = 1V$$

$$I_E \approx I_C = 1.2mA$$

$$V_E = I_E R_E$$

$$R_E = V_E / I_E = 1V / 1.2mA$$

$$R_E = 833.33\Omega$$

Choose, $R_E = 800\Omega$

$$V_{CC} = I_C R_C + V_{CE} + V_E$$

$$R_C = (V_{CC} - V_{CE} - V_E) / I_C = (10 - 5 - 1) / 1.2mA$$

$$R_C = 3.3k\Omega$$

Choose, $R_C = 3.9k\Omega$

$$V_{BE} = V_B - V_E$$

$$V_B = V_{BE} + V_E = 0.7 + 1 = 1.7V$$

$$V_B = (V_{CC} * R_2) / (R_1 + R_2) = 15k\Omega$$

$$R_2 / (R_1 + R_2) = 1.7 / 10 = 0.17$$

$$R_1 = 15k\Omega / 0.17 = 88.24k\Omega$$

Choose, $R_1 = 100k\Omega$

$$R_2 / (R_1 + R_2) = 0.17$$

$$R_2 = 18k\Omega$$

Choose, $R_2 = 12k\Omega$

Let $C_1 = C_2 = 0.1\mu F$

PROCEDURE:

1. Connect the circuit as per the circuit diagram.
2. For the Colpitts oscillator adjust the capacitance in the tank circuit to get a sinusoidal signal of desired frequency
3. Plot the output obtained in the linear graph.

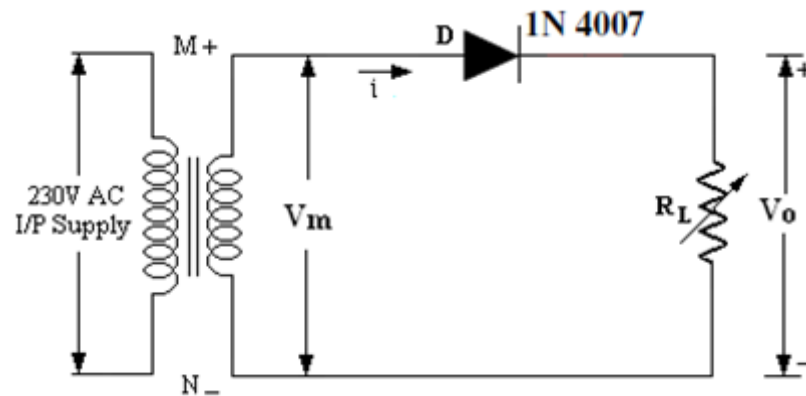
REVIEW QUESTIONS:

1. Which oscillator is very suitable for radio frequency range applications?
2. Why are Colpitts oscillators used to generate fixed radio-frequency signals?
3. What are the advantages and disadvantages of Hartley and colpitts oscillator?
4. Name two high frequency Oscillators.
5. What are the essential parts of an Oscillator
6. How does an oscillator differ from an amplifier?
7. Name two low frequency oscillators?
8. What are the classifications of Oscillators?
9. State the frequency for LC phase shift oscillator?
10. How does a Colpitt's oscillator differ from Hartley oscillator?
11. How is frequency of oscillations determined?
12. State few applications of Colpitt's oscillator.
13. State the typical operating range of Colpitt's oscillator.
14. What is the role of decoupling capacitor?
15. What is the total phase shift that occurs in Colpitt's oscillator?

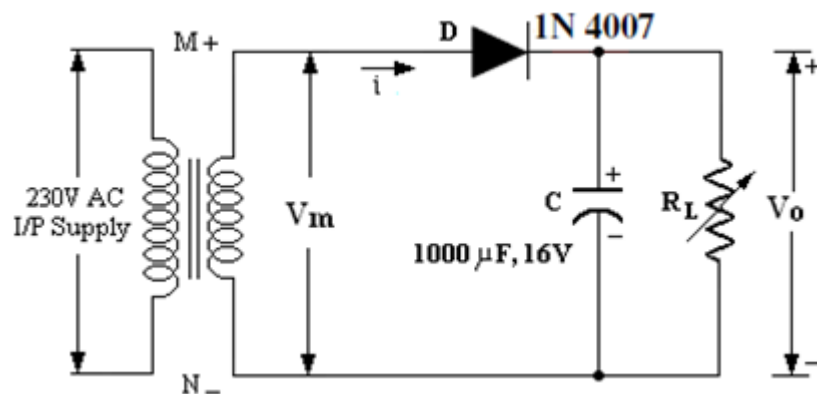
RESULT:

Thus Colpitts oscillator is designed and constructed, and the output sine wave form is observed and compared with theoretical oscillation frequency.

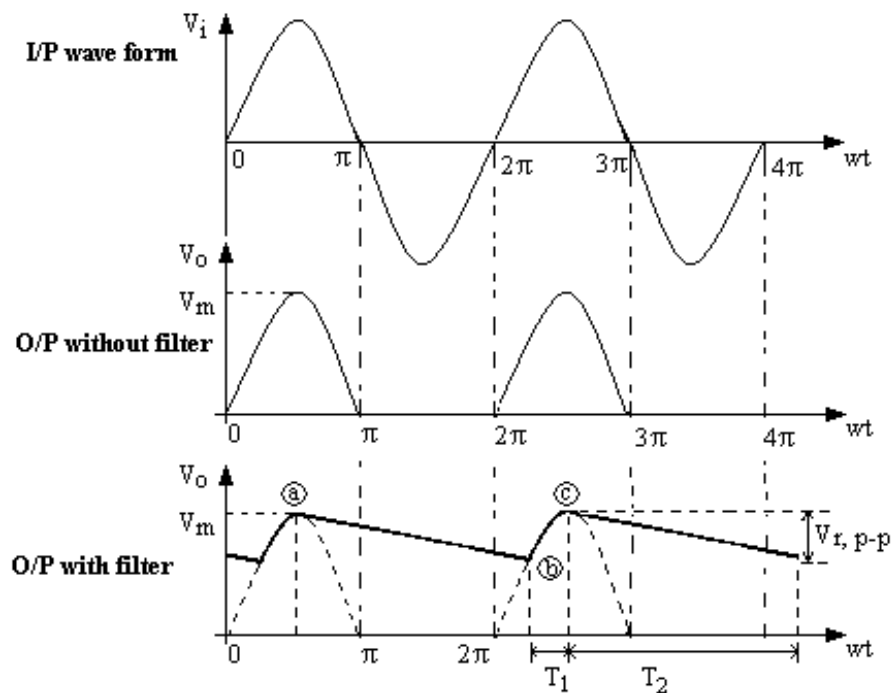
CIRCUIT DIAGRAM FOR HALF WAVE RECTIFIER WITHOUT FILTER:



CIRCUIT DIAGRAM FOR HALF WAVE RECTIFIER WITH FILTER:



Half-wave Rectifier waveforms without and with Filter



Ex. No.: 9(a)

HALF WAVE RECTIFIER

AIM:

To Rectify the AC signal and then to find out Ripple factor and percentage of Regulation in Half wave rectifier with and without Capacitor filter.

APPARATUS REQUIRED:

Sl. No	Components / Equipments	Specifications	Quantity
1	Transformer	230V/(12-0-12) V	1
2	Diode	1N4007	1
3	Capacitors	1000 μ F,16V/470 μ F/ 25V	1
4	Decade Resistance Box/ Resistor	- / 10k Ω	1
5	Dual Trace CRO	20MHz	1
6	Multimeter		1
7	Bread Board		1
8	Connecting Wires		Few

THEORY

In half wave rectifier only one diode is used which conducts during positive cycle. During positive half cycle of the input voltage anode of the diode is positive compared with the cathode. Diode is in forward bias and current passes through the diode and positive cycle develops across the load resistance R_L . During negative half cycle of input voltage, anode is negative with respected to cathode and diode is in reverse bias. No current passes through the diode hence output voltage is zero.

Half wave rectifier without filter capacitor convert AC voltage into pulsating DC voltage. Filter capacitor is used to obtain smooth DC voltage. For practical circuits, transformer coupling is usually provided for two reasons.

- ✓ The voltage can be stepped-down, as needed.
- ✓ The AC source is electrically isolated from the rectifier. Thus, preventing shock hazards in the secondary circuit.

TABULATION WITHOUT FILTER:

V no load Voltage (Vdc) = V

Load Resistance $R_L (\Omega)$	O/P Voltage (Vo)		Ripple factor $\gamma = \frac{V_{ac}}{V_{dc}}$
	$V_{ac} (V)$	$V_{dc} (V)$	

TABULATION WITH FILTER:

V no load Voltage (Vdc) = V

Load Resistance $R_L (\Omega)$	O/P Voltage (Vo)		Ripple factor $\gamma = \frac{V_{ac}}{V_{dc}}$
	$V_{ac} (V)$	$V_{dc} (V)$	

PROCEDURE:

Without Capacitor:

1. Test your transformer: Give 230V, 50Hz source to the primary coil of the transformer and observe the AC waveform of rated value without any distortion at the secondary of the transformer.
2. Connect the half wave rectifier as shown in figure.
3. Measure the V_{dc} & V_{ac} using DC and AC Voltmeters.
4. Calculate the ripple factor $r = V_{ac} / V_{dc}$
5. Compare the theoretical ripple factor with the practical ripple factor.

With capacitor:

1. Connect the half wave rectifier with filter circuit as shown in fig.
2. Connect CRO across load.
3. Keep the CRO switch in ground mode and observe the horizontal line and adjust it to the X-axis.
4. Switch the CRO into DC mode and observe the waveform.

Calculations:

Without Filter:

R_F = Forward resistance of diode = 30Ω

R_L = Load resistance

$$V_{dc} = \frac{V_m R_L}{\pi(R_F + R_L)}$$

$$V_{rms} = \frac{V_m R_L}{2(R_F + R_L)}$$

$$\text{Ripple factor} = r = \frac{V_{rms}}{V_{dc}}$$

Average load voltage at no load (V_{NL}) = V_m/π

Average load voltage at full load = $V_{FL} = \frac{V_m R_L}{2(R_F + R_L)}$

With Filter:

$f = 50\text{Hz}$

$$V_{dc} = \frac{V_m R_L}{\frac{1}{4fC} + R_L}$$

$$V_{rms} = \left(\frac{1}{2\sqrt{3}fC} \right) \left(\frac{V_m}{\frac{1}{4fC} + R_L} \right)$$

$$\text{Ripple factor} = r = \frac{V_{rms}}{V_{dc}} = \frac{V_{ac}}{V_{dc}} \times 100\%$$

Calculate Percentage of Regulation, $\eta = \frac{V_{no\ load} - V_{full\ load}}{V_{no\ load}} \times 100\%$

=

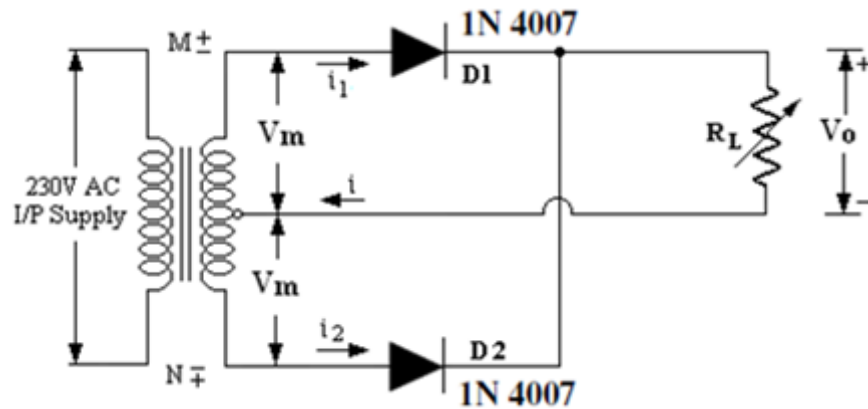
REVIEW QUESTIONS

1. What is a rectifier? Mention the applications of rectifier.
2. Compare and List the various types of Rectifiers.
3. What are advantages and disadvantages of half-wave rectifier?
4. How Diode acts as a rectifier?
5. What is the significance of PIV? What is the condition imposed on PIV?
6. What is meant by ripple factor (γ)? For a good filter whether ripple factor should be high or low?
7. What is meant by regulation?
8. What happens to the output wave form if we increase the capacitor value?
9. A half-wave rectifier circuit with a capacitive filter is connected to 200 Volts, 50 Hz ac line. What will be the output voltage across the capacitor?
10. What is the mathematical relationship between rms input AC voltage and DC output voltage in half wave rectifier with and without filter capacitor?

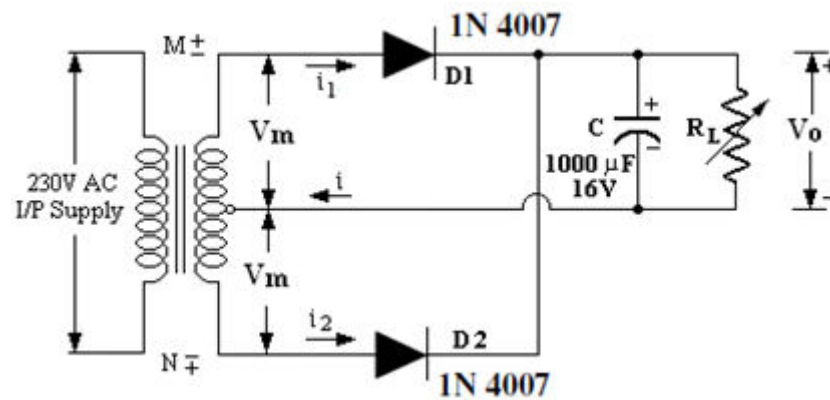
RESULT:

Thus the half wave rectifier is designed with and without capacitor filter and the corresponding dc output voltages and the ripple factors are measured and verified with the theoretical values.

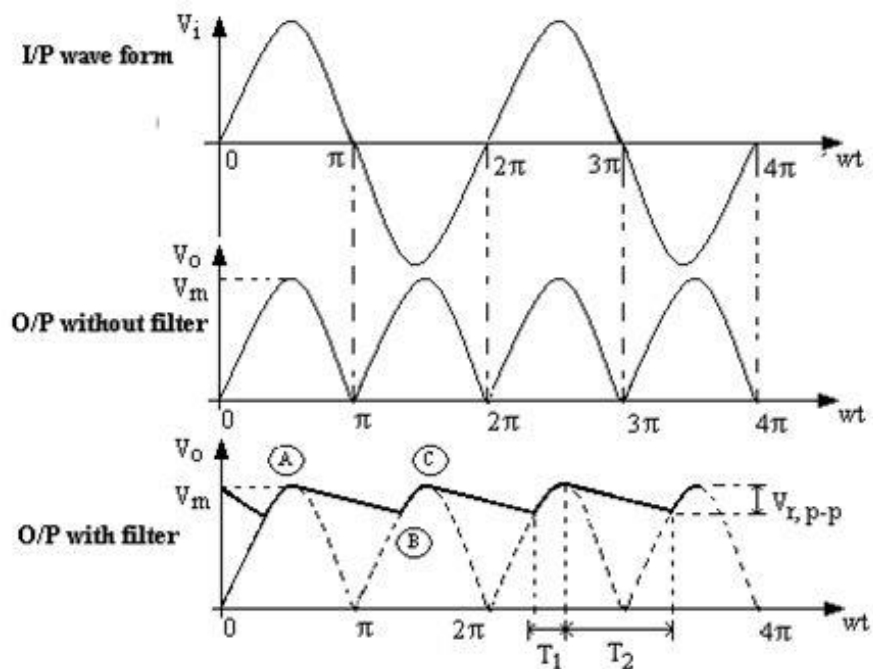
CIRCUIT DIAGRAM FOR FULL WAVE RECTIFIER WITHOUT FILTER:



CIRCUIT DIAGRAM FOR FULL WAVE RECTIFIER WITH FILTER:



FULL-WAVE RECTIFIER WAVEFORMS WITHOUT AND WITH FILTER



Ex. No.: 9(b)

FULL WAVE RECTIFIER

AIM:

To Rectify the AC signal and then to find out Ripple factor and percentage of Regulation in Full wave center tapped rectifier with and without Capacitor filter.

APPARATUS REQUIRED:

Sl. No	Components / Equipments	Specifications	Quantity
1	Transformer	230V/(12-0-12) V	1
2	Diode	1N4007	2
3	Capacitors	1000 μ F,16V/ 470 μ F,25V	1
4	Decade Resistance Box/ Resistor	- / 10k Ω	1
5	Dual Trace CRO	20MHz	1
6	Multimeter	-	1
7	Bread Board		1
8	Connecting Wires		Few

THEORY

Full wave rectifier utilizes both the cycle of input AC voltage. Two or four diodes are used in full wave rectifier. If full wave rectifier is designed using four diodes it is known as full wave bridge rectifier. Full wave rectifier using two diodes without capacitor is shown in the figure. Center tapped transformer is used in this full wave rectifier. During the positive cycle diode D1 conducts and it is available at the output. During negative cycle diode D1 remains OFF but diode D2 is in forward bias hence it conducts and negative cycle is available as a positive cycle at the output. Note that direction of current in the load resistance is same during both the cycles hence output is only positive cycles.

Advantages of full wave rectifier over half wave rectifier:

- ✓ The rectification efficiency is double than half wave rectifier
- ✓ Ripple factor is less and ripple frequency is double hence easy to filter out.
- ✓ DC output voltage and current is higher hence output power is higher.
- ✓ Better transformer utilization factor
- ✓ There is no DC saturation of core in transformer because the DC currents in two halves of secondary flow in opposite directions.

Disadvantages:

- ✓ Requires center tap transformer
- ✓ Requires two diodes compared to one diode in half wave rectifier.

TABULATION WITHOUT FILTER:

V no load Voltage (Vdc) = V

Load Resistance $R_L (\Omega)$	O/P Voltage (Vo)		Ripple factor $\gamma = \frac{V_{ac}}{V_{dc}}$
	$V_{ac} (V)$	$V_{dc} (V)$	

TABULATION WITH FILTER:

V no load Voltage (Vdc) = V

Load Resistance $R_L (\Omega)$	O/P Voltage (Vo)		Ripple factor $\gamma = \frac{V_{ac}}{V_{dc}}$
	$V_{ac} (V)$	$V_{dc} (V)$	

PROCEDURE:

WITHOUT FILTER:

1. Connecting the circuit on bread board as per the circuit diagram.
2. Connect the primary of the transformer to main supply i.e. 230V, 50Hz
3. Connect the decade resistance box and set the RL value to 100Ω
4. Connect the Multimeter at output terminals and vary the load resistance (DRB)
5. from 100Ω to $1K\Omega$ and note down the V_{ac} and V_{dc} as per given tabular form
6. Disconnect load resistance (DRB) and note down no load voltage V_{dc} (V no load)
7. Connect load resistance at $1k\Omega$ and connect Channel – II of CRO at output terminals and CH – I of CRO at Secondary Input terminals observe and note down the Input and Output Wave form on Graph Sheet.
8. Calculate ripple factor $\gamma = \frac{V_{ac}}{V_{dc}}$
9. Calculate Percentage of Regulation, $\% \eta = \frac{V_{no\ load} - V_{full\ load}}{V_{no\ load}} \times 100\%$

WITH CAPACITOR FILTER:

1. Connecting the circuit as per the circuit Diagram and repeat the above procedure from steps 2 to 8.

Calculations:

Without Filter:

R_F = Forward resistance of diode = 30Ω

R_L = Load resistance

$$V_{dc} = \frac{V_m R_L}{\pi(R_F + R_L)}$$

$$V_{rms} = \frac{V_m R_L}{2(R_F + R_L)}$$

$$\text{Ripple factor} = r = \frac{(V_{rms}^2 - V_{dc}^2)^{1/2}}{V_{dc}}$$

Average load voltage at no load (V_{NL}) = V_m/π

Average load voltage at full load = $V_{FL} = \frac{V_m R_L}{2(R_F + R_L)}$

With Filter:

$f = 50\text{Hz}$

$$V_{dc} = \frac{V_m R_L}{\frac{1}{4fC} + R_L}$$

$$V_{rms} = \left(\frac{1}{2\sqrt{3}fC}\right) \left(\frac{V_m}{\frac{1}{4fC} + R_L}\right)$$

Calculate Percentage of Regulation, $\% \frac{V_{dc} - V_{dc}}{V_{dc}} = \frac{V_{dc} - V_{dc}}{V_{dc}} \times 100\%$

Ripple factor = $r = V_{rms} / V_{dc} \text{ (or) } \gamma = \frac{V_{rms}}{V_{dc}} \times 100\%$

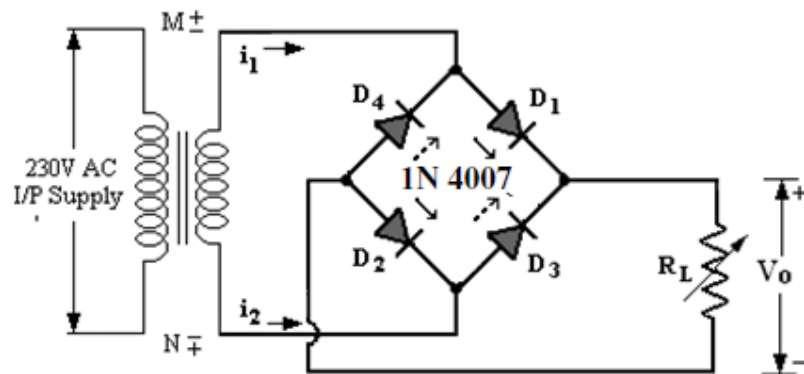
REVIEW QUESTIONS

1. What is a full wave rectifier?
2. Compare capacitor filter with an inductor filter?
3. What is meant by regulation? Why regulation is poor in the case of inductor filter?
4. What is meant by time constant?
5. What is the frequency of AC component at the output of full wave rectifier? Give reason.
6. What is the difference in DC output voltage in half wave and full wave rectifier for the same AC input?
7. What is the PIV necessary for the diode if transformer of 24-0-24 V is used?
8. What is the mathematical relationship between rms input AC voltage and DC output voltage in half wave rectifier with and without filter capacitor?
9. Compare the efficiency of full wave Bridge Rectifier with Half wave Rectifier.
10. Measure the DC component in the output by varying the C value in the Filter.

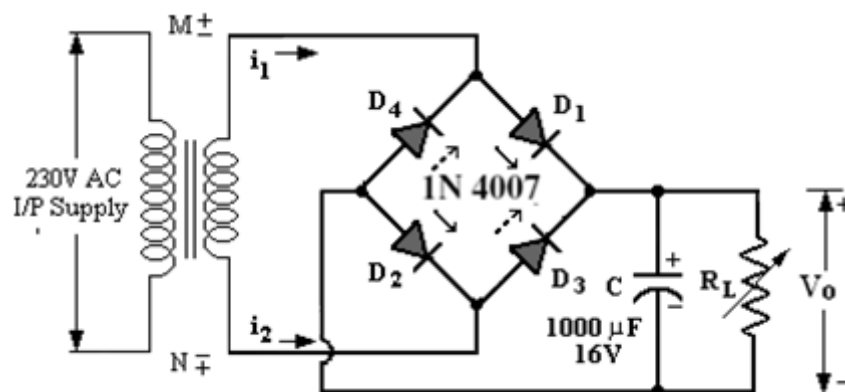
RESULT:

Thus the Full wave rectifier is designed with and without capacitor filter and the corresponding dc output voltages and the ripple factors are measured and verified with the theoretical values.

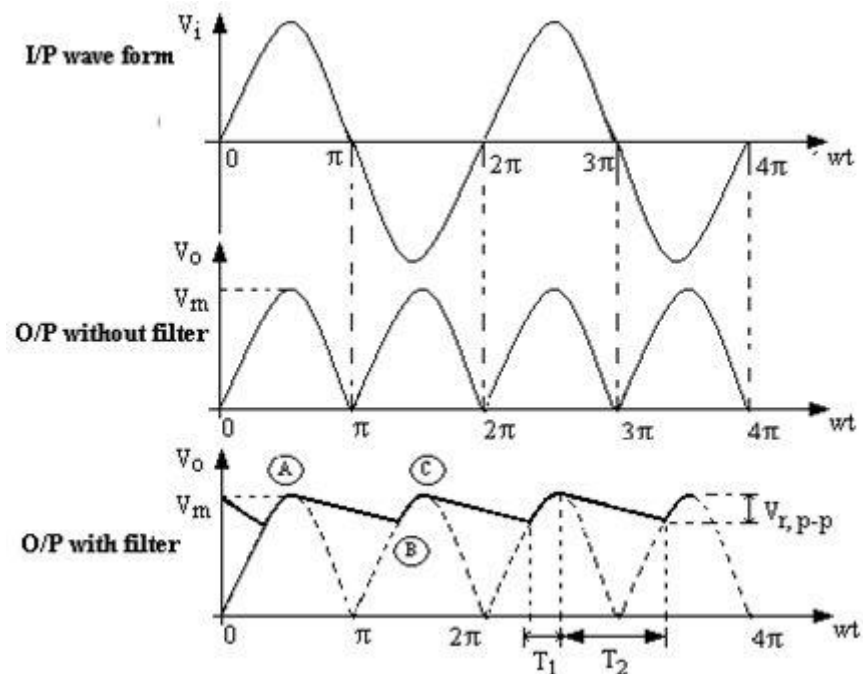
CIRCUIT DIAGRAM FOR FULL WAVE RECTIFIER WITHOUT FILTER:



CIRCUIT DIAGRAM FOR FULL WAVE RECTIFIER WITH FILTER:



Full-wave Rectifier waveforms without and with Filter



Ex. No.: 9(c)

FULL WAVE BRIDGE RECTIFIER

AIM:

To Rectify the AC signal and then to find out Ripple factor and percentage of Regulation in Full-wave Bridge rectifier circuit with and without Capacitor filter.

APPARATUS REQUIRED:

Sl. No	Components / Equipments	Specifications	Quantity
1	Transformer	230V/(12-0-12) V	1
2	Diode	1N4007	4
3	Capacitors	1000 μ F,16V/ 470 μ F,25V	1
4	Decade Resistance Box/ Resistor	- / 10k Ω	1
5	Dual Trace CRO	20MHz	1
6	Multimeter		1
7	Bread Board		1
8	Connecting Wires		Few

THEORY:

The Bridge rectifier is a circuit, which converts an AC voltage to DC voltage using both half cycles of the input AC voltage. The circuit has four diodes connected to form a bridge. The ac input voltage is applied to the diagonally opposite ends of the bridge. The load resistance is connected between the other two ends of the bridge. For the positive half cycle of the input ac voltage, diodes D1 and D2 conduct, whereas diodes D3 and D4 remain in the OFF state. The conducting diodes will be in series with the load resistance R_L and hence the load current flows through R_L . For the negative half cycle of the input ac voltage, diodes D3 and D4 conduct whereas, D1 and D2 remain OFF. The conducting diodes D3 and D4 will be in series with the load resistance R_L and hence the current flows through R_L in the same direction as in the previous half cycle. Thus a bi-directional wave is converted into a unidirectional wave.

TABULATION WITHOUT FILTER:

V no load Voltage (V_{dc}) = V

Load Resistance $R_L (\Omega)$	O/P Voltage (V _o)		Ripple factor $\gamma = \frac{V_{ac}}{V_{dc}}$
	V _{ac} (V)	V _{dc} (V)	

TABULATION WITH FILTER:

V no load Voltage (V_{dc}) = V

Load Resistance $R_L (\Omega)$	O/P Voltage (V _o)		Ripple factor $\gamma = \frac{V_{ac}}{V_{dc}}$
	V _{ac} (V)	V _{dc} (V)	

Advantages of bridge rectifier:

- ✓ No center tap is required in the transformer secondary hence transformer design is simple. If stepping up and stepping down not required than transformer can be eliminated. (In SMPS used in TV and computer, 230V is directly applied to the input of bridge rectifier). The PIV of the diode is half than in center tap full wave rectifier.
- ✓ Transformer utilization factor is higher than in center tapped full wave rectifier.
- ✓ Smaller size transformer required for given capacity because transformer is utilized effectively during both AC cycles.

Disadvantages of bridge rectifier:

- ✓ Requires Four diodes (But package is low cost)
- ✓ Forward voltage drop across two diodes. This will reduce efficiency particularly when low voltage (less than 5V) is required.
- ✓ Load resistance and supply source have no common point which may be earthed.

PROCEDURE:

WITHOUT FILTER:

1. Connecting the circuit on bread board as per the circuit diagram.
2. Connect the primary of the transformer to main supply i.e. 230V, 50Hz
3. Connect the decade resistance box and set the RL value to 100 Ω
4. Connect the Multimeter at output terminals and vary the load resistance (DRB)
5. from 100 Ω to 1K Ω and note down the Vac and Vdc as per given tabular form
6. Disconnect load resistance (DRB) and note down no load voltage Vdc (V no load)
7. Connect load resistance at 1K Ω and connect Channel – II of CRO at output terminals and CH – I of CRO at Secondary Input terminals observe and note down the Input and Output Wave form on Graph Sheet.
8. Calculate ripple factor $\gamma = \frac{V_{ac}}{V_{dc}}$
9. Calculate Percentage of Regulation, $\% \eta = \frac{V_{no\ load} - V_{full\ load}}{V_{no\ load}} \times 100\%$

WITH CAPACITOR FILTER:

1. Connecting the circuit as per the circuit Diagram and repeat the above procedure from steps 2 to 8.

CALCULATIONS:

Without Filter:

R_F = Forward resistance of diode = 30Ω

R_L = Load resistance

$$V_{dc} = \frac{V_m}{\pi}$$
$$V_{rms} = \frac{V_m}{\sqrt{2}}$$

$$\text{Ripple factor} = r = \left(\frac{V_{rms}^2 - V_{dc}^2}{V_{dc}^2} \right)^{1/2}$$

2.

Average load voltage at no load (V_{NL}) = $2V_m/\pi$

Average load voltage at full load = $V_{FL} = \frac{2V_m R_L}{\pi(2R_F + R_L)}$

With Filter:

$f = 50\text{Hz}$

$$V_{dc} = \frac{V_m R_L}{\frac{1}{4fC} + R_L}$$
$$V_{rms} = \left(\frac{1}{4\sqrt{3}fC} \right) \left(\frac{V_m}{\frac{1}{4fC} + R_L} \right)$$

$$\text{Ripple factor} = r = V_{rms} / V_{dc} \quad (\text{Or}) \quad \gamma = \frac{V_{ac}}{V_{dc}}$$

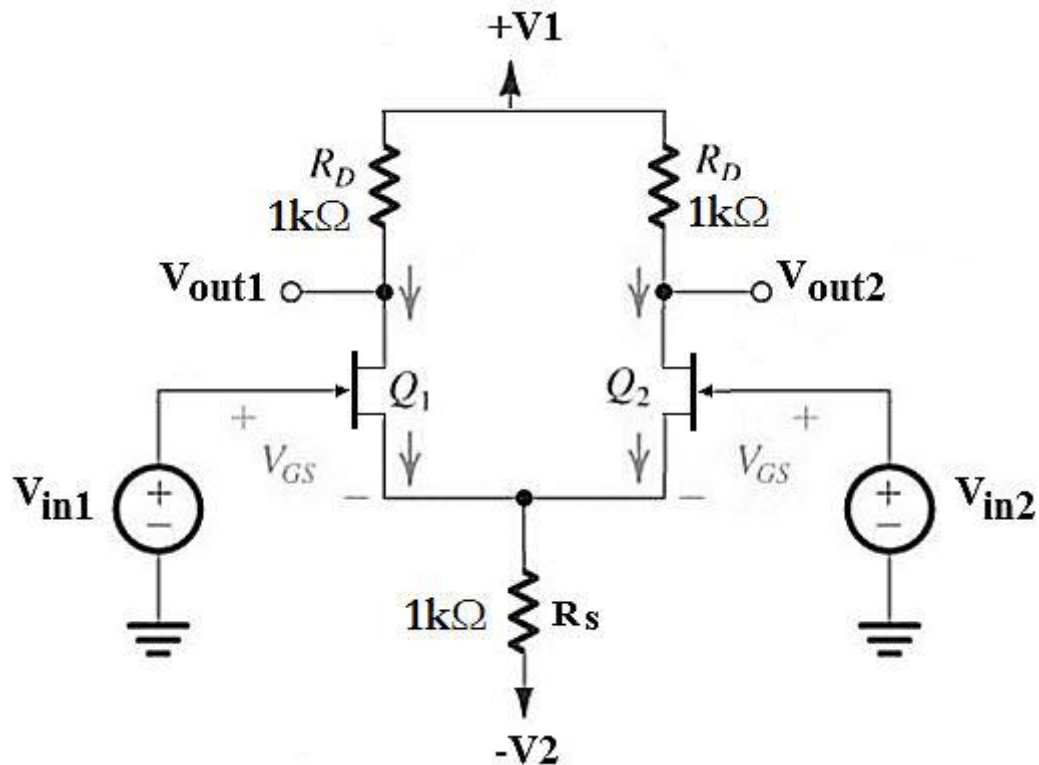
REVIEW QUESTIONS:

1. What are the advantages of Bridge Rectifier over the center tapped Rectifier?
2. What is the efficiency of bridge rectifier?
3. In filters capacitor is always connected in parallel, why?
4. If the output voltage of a bridge rectifier is 100V, the PIV of diode will be?
5. What does Regulation indicate?
6. What is the Theoretical maximum value of Ripple factor of a Full-wave Rectifier?
7. What is the PIV requirement of a Diode in a Bridge Rectifier?
8. Explain the operation of Bridge Rectifier.
9. Mention the TUF for the Centre tapped Rectifier.
10. How will you choose the transformer for a rectifier circuit.

RESULT:

Thus the Full wave bridge rectifier is designed with and without capacitor filter and the corresponding dc output voltages and the ripple factors are measured and verified with the theoretical values.

CIRCUIT DIAGRAM:



MODEL CALCULATIONS:

i) For common mode signal:

$$V_1 = \quad \text{volts}$$

$$V_2 = \quad \text{volts}$$

$$\text{Gain } A_c = V_o / ((V_1 + V_2) / 2)$$

$$A_c =$$

ii) For differential mode signal:

$$V_1 = \quad \text{volts}$$

$$V_2 = \quad \text{volts}$$

$$\text{Gain } A_d = V_o / (V_1 - V_2)$$

$$A_d =$$

$$\text{CMRR in dB} = 20 \log_{10}(A_d / A_c).$$

Ex. No.: 10

DIFFERENTIAL AMPLIFIERS USING FET

AIM:

To construct the Differential Amplifier in Differential mode and to find the common mode rejection ratio (CMRR).

APPARATUS REQUIRED:

Sl. No	Components / Equipments	Specifications	Quantity
1	FET	BFW10	2
2	Resistor	1k Ω	3
3	Dual Trace CRO	20MHz	1
4	Dual Regulated Power Supply	(0-30)V	1
5	Bread Board		1
6	Connecting Wires		Few

THEORY:

A differential amplifier is a type of electronic amplifier that amplifies the difference between two input voltages but suppresses any voltage common to the two inputs. Differential amplifiers are usually implemented with a basic two-transistor circuit called a long-tailed pair or differential pair. This circuit was originally implemented using a pair of vacuum tubes. The circuit works the same way for all three-terminal devices with current gain. The long-tail resistor circuit bias points are largely determined by Ohm's Law and less so by active component characteristics.

FORMULA:

$$\text{C.M.R.R} = | A_d / A_c |$$

$$\text{C.M.R.R in dB} = 20 \log | A_d / A_c |$$

A_d = Differential mode gain

A_c = Common mode gain

PROCEDURE:

1. Connections are made as per the circuit diagram.
2. Switch ON the RPS
3. Vary the input voltages using function generator and note the corresponding output voltage.
4. Reduce the RPS voltage to 0 V
5. Calculate the Gain.
6. Calculate the CMRR

REVIEW QUESTIONS:

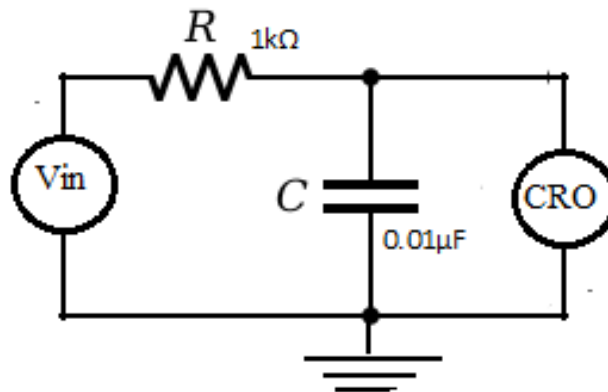
1. What is Differential amplifier?
2. What is difference between amplifier and Differential amplifier?
3. Sketch the circuit diagram of Differential amplifier using BJT.
4. List out the applications of Differential amplifier.
5. What is the mode of operations in Diff. Amp?
6. What is Common mode gain and difference mode gain?
7. What is the use of CMRR?
8. What is gain?
9. What is the unit of current and voltage gain?
10. Compare the application of Differential amplifier using FET with Diff. Amp using BJT.

RESULT:

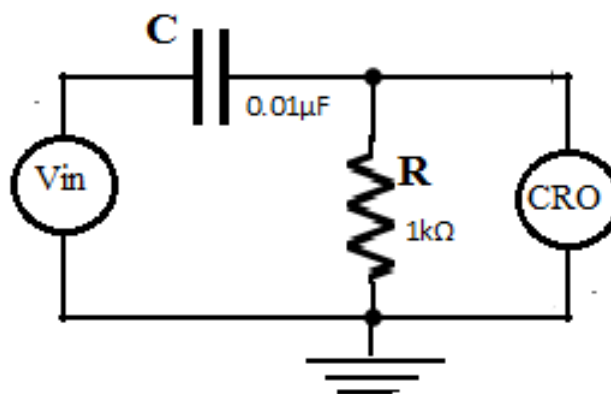
Thus the differential amplifier is constructed and CMRR has been calculated.

CIRCUIT DIAGRAM

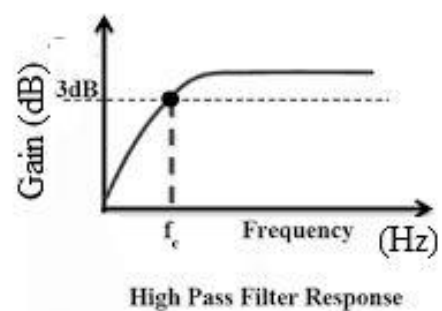
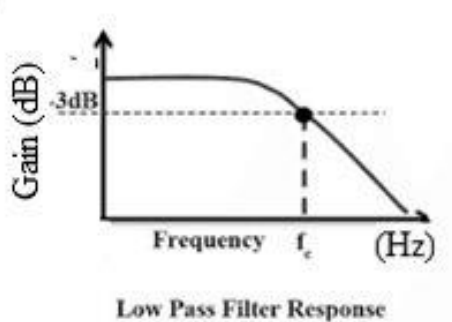
LOW PASS FILTER:



HIGH PASS FILTER:



MODEL GRAPH:



Ex. No.: 11

REALIZATION OF PASSIVE FILTERS

AIM:

To realize the characteristics of passive low pass filter and high pass filter.

APPARATUS REQUIRED:

Sl. No	Components / Equipments	Specifications	Quantity
1	Function Generator	(0- 20MHz)	1
2	Capacitors	0.01 μ F	1
3	Resistor	1k Ω	1
4	Dual Trace CRO	(0- 20MHz)	1
6	Bread Board		1
7	Connecting Wires		Few

THEORY:

Passive filters are made up of passive components such as resistors, capacitors and inductors and have no amplifying elements (transistors, op-amps, etc.) so have no signal gain, therefore their output level is always less than the input. At low frequencies the reactance of the capacitor will be very large than the resistors resistive value. So, the signal's voltage potential across capacitor will be much larger than the voltage drop across the resistor. In higher frequencies exact opposite thing will happen. Resistor's resistive value gets higher and due to that with the effect of capacitor's reactance the voltage across capacitor became smaller. Filters are so named according to the frequency range of signals that they allow to pass through them, while blocking or "attenuating" the rest.

The most commonly used filter designs are:

The Low Pass Filter – the low pass filter only allows low frequency signals from 0Hz to its cut-off frequency, f_c point to pass while blocking those any higher. The High Pass Filter – the high pass filter only allows high frequency signals from its cut-off frequency, f_c point and higher to infinity to pass through while blocking those any lower.

DESIGN:

$$\text{Cut off frequency } f_c = \frac{1}{2\pi RC}$$

Given $f = 15\text{kHz}$ and $C = 0.01\mu\text{F}$

$$R = \frac{1}{2\pi f C} = 1.06\text{k}\Omega \cong 1\text{k}\Omega$$

TABULATION:**(i) Low Pass Filter** $V_{in} =$ (volts)

Frequency (Hz)	Vout (Volts)	$Gain - 20\log_{10}\left(\frac{V_{out}}{V_{in}}\right)$ dB

(ii) High Pass Filter

Frequency (Hz)	Vout (Volts)	$Gain - 20\log_{10}\left(\frac{V_{out}}{V_{in}}\right)$ dB

PROCEDURE:

1. Connect the components as per the circuit diagram in the breadboard.
2. Set the input sinusoidal signal of 5Vots in the function generator.
3. Vary the frequency and note down the output voltage in the CRO.
4. Find the gain and plot the frequency response of the filter from which determine the cut off frequency of the filter designed.

REVIEW QUESTIONS:

1. What is a passive filter?
2. Differentiate Active filter and Passive Filter.
3. What is the roll off rate of the frequency response obtained from the filter designed?
4. Classify the filter types.
5. Why 3dB line is drawn to fine the bandwidth of a filter?

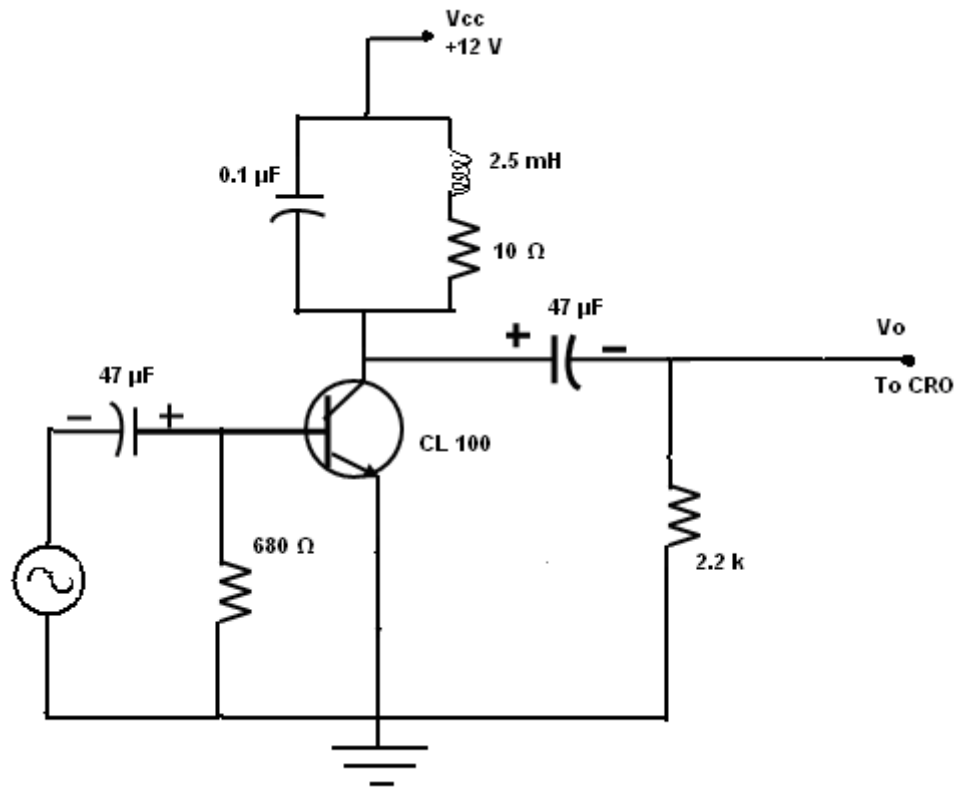
RESULT:

Thus the frequency response of the passive low pass and high pas filter is obtained.

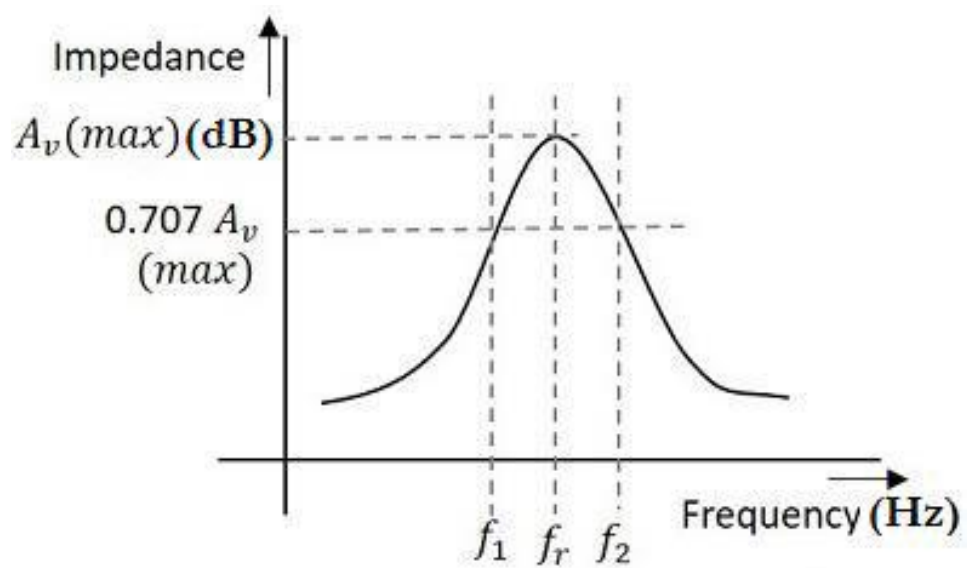
Filter Type	Low Pass Filter	High Pass Filter
Theoretical cut off frequency		
Practical cut off frequency		

TUNED CLASS C AMPLIFIER:

CIRCUIT DIAGRAM:



MODEL GRAPH:



Ex. No.: 12

TUNED CLASS C AMPLIFIER

AIM:

To design and construct the class-c power amplifier and to plot its frequency response.

APPARATUS REQUIRED:

Sl. No	Components / Equipments	Specifications	Quantity
1	Transistor	BC107	1
2	Resistor	4.2K Ω , 500 Ω , 197K Ω , 2.2K Ω ,	Each One
3	Capacitors	0.1 μ f 0.001 μ f, 100 μ f	2 1
4	Decade Inductance Box	-	1
5	Dual Trace CRO	(0- 20MHz)	1
6	Regulated Power Supply	(0-30) V	1
7	Function Generator	20MHz	1
8	Bread Board		1
9	Connecting Wires		Few

THEORY:

In a class-c amplifier, the transistor is in the active region for less than half cycle. It means, conduction takes place for less than one half cycle. This implies that the collector current of a class-c amplifier is highly non-sinusoidal because current flows in pulses. The load is a tuned circuit which converts the non-sinusoidal o/p to nearly sinusoidal form. Because of the flow of collector current less than 180°, the average collector current is much less, if hence losses are less, so efficiency is very high.

$$\text{Resonance frequency } (f_r) = 1/2\pi\sqrt{LC}.$$

At resonant frequency, the inductance of parallel resonant circuit is very high and is purely resistive. When the circuit is tuned to the resonant frequency, the voltage across R_1 is maximum and sinusoidal. The tuned circuit helps in rejecting the harmonics that are developed in the transistor due to class-C operation.

The class-c tuned power amplifier consists of an LC tuned circuit in the collector of Q. R_1 & R_2 provides the necessary biasing for Q. C_1 & C_3 are the i/p and o/p coupling capacitors. The Q point is kept just above the cut-off line on the dc load line. R_L is provided to load the amplifier.

OBSERVATION:

V _{in} =____(v)		
Frequency(Hz)	V _{out} (v)	Gain(dB)=20 log(V ₀ /V _{in})

PROCEDURE:

1. Connect the circuit as for circuit diagram
2. Calculate the theoretical resonant frequency $f_r = \frac{1}{2\pi\sqrt{LC}}$
3. Connect the input signal to the amplifier.
4. Keep input voltage zero initially and adjust frequency to around resonance frequency (f_r)
5. Observe the output waveform increase the input ac voltage until we get the maximum distorted output.
6. Vary the frequency in required steps surrounding resonant frequency and note down the corresponding output voltages & calculate gain.
7. Plot the graph between gain and frequency.

REVIEW QUESTIONS:

1. What is tuned amplifier? What are the various types of tuned amplifiers?
2. Why tuned amplifier cannot be used at low frequency?
3. What is the other name for tuned amplifier?
4. Mention the applications of tuned amplifiers.
5. State advantages and disadvantages of tuned amplifiers.
6. Compare amplifier, feedback amplifier & tuned amplifier.
7. List out the different coil losses.
8. What are the different types of neutralization?
9. What is the need for neutralization circuits?
10. Define loaded and unloaded Q.

RESULT:

Thus single tuned amplifier is designed and constructed for the given operating frequency and the frequency response is plotted.

